



Ain Shams University
Faculty of Engineering
Electric Power and Machine Department

Transformerless Dynamic Voltage Restorer for Medium Voltage Distribution Networks

M.Sc. thesis

by:

Eng. Ayman Bahgat Abd-El-Azim Ibrahim

A thesis submitted to the Faculty of Engineering –Ain Shams University
in partial fulfillments of the requirements for the M.Sc. degree in
Electrical Power and Machines Engineering

Supervised by:

Prof Dr. Ahmed Abd-El-Sattar Abd-El-Fattah

Electric Power and Machines Department
Faculty of Engineering, Ain Shams University

Dr. Mostafa Ibrahim Mohamed Marei

Electric Power and Machines Department
Faculty of Engineering, Ain Shams University

Cairo 2009

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

APPROVAL SHEET

For the M.Sc. Thesis:

Transformerless Dynamic Voltage Restorer for Medium Voltage Distribution Networks

by:

Eng. Ayman Bahgat Abd-El-Azim Ibrahim

**A thesis submitted to the Faculty of Engineering –Ain
Shams University in partial fulfillments of the requirements
for the M.Sc. degree in Electrical Power and Machines
Engineering**

Approved by

Name

Signature

Prof. Dr. Ahmed Abd-El-Sattar Abd-El-Fattah

Electric Power and Machine Department
Faculty of Engineering- Ain Shams University

Dr. Mostafa Ibrahim Mohamed Marei

Electric Power and Machine Department
Faculty of Engineering- Ain Shams University

EXAMINERS COMMITTEE

For the M.Sc. Thesis:

**Transformerless Dynamic Voltage Restorer
for Medium Voltage Distribution Networks**

by:

Eng. Ayman Bahgat Abd-El-Azim Ibrahim

**A thesis submitted to the Faculty of Engineering –Ain
Shams University in partial fulfillments of the requirements
for the M.Sc. degree in Electrical Power and Machines
Engineering**

Name, title and affiliation

Signature

Prof. Dr. Abbas Aly El Hefnawy

President of Delta University for Science and Technology

Prof. Dr. Ahmed Mohammed Asaad Mahmoud

Head of Electric Power and Machines Department

Faculty of Engineering- Ain Shams University

Prof. Dr. Ahmed Abd-El-Sattar Abd-El-Fattah

Electric Power and Machine Department

Faculty of Engineering- Ain Shams University

STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for M.Sc. degree in Electrical Engineering.

The included work in this thesis has been carried out by the author at the Electrical Power and Machine Department, Ain Shams University. No part of this thesis has been submitted for a degree or a qualification at any other university or institution.

Name: Ayman Bahgat Abd-El-Azim Ibrahim

Signature:

Date:

ACKNOWLEDGEMENTS

First of all, I am much thankful to Allah. I would like to express my deepest gratitude and thankfulness to Prof. Dr. Ahmed Abd-El-Sattar Abd-El-Fattah and Dr. Mostafa Ibrahim M. Marei for their great support, excellent supervision and encouragement shown during the period of this study.

Special thanks to the Electrical Power and Machines Department, Faculty of Engineering; Ain Shams University, for their great support.

ABSTRACT

Voltage disturbances are the most common power quality problems causing effects ranging from minor annoyance through equipment failure to the shutdown of complete production processes. The economic impact can be very large and can threaten the economic viability of a business. The Dynamic Voltage Restorer (DVR) is considered as the most effective and economic solution for all types of voltage disturbances.

This thesis introduces a proposed transformerless DVR structure that is suitable for medium voltage distribution networks. The proposed control system is capable of compensating all types of voltage disturbances like voltage sags, voltage swells, voltage flickers and long duration voltage variations; the disturbance compensation is done with minimum energy requirements.

The proposed DVR system is based on cascaded H-bridge multilevel inverter topology which enables to eliminate the insertion transformer; hence the cost and size of the DVR are effectively reduced. Different PWM switching techniques are discussed and simulated using the EMTDC/PSCAD simulation package. Simulation results are compared in order to adopt the best switching technique for the cascaded H-bridge multilevel inverter. Different compensating techniques are studied and simulated to demonstrate the advantages and disadvantages of each method.

The dynamic performance of the proposed transformerless DVR is studied which validate the accuracy of the proposed control technique. The ability of the proposed transformerless DVR to compensate voltage disturbance with minimum energy requirements is proved by using capacitors as energy storage elements instead of dc power supplies.

The proposed minimum energy control technique of the DVR is shown to be superior in terms of lower storage energy need and efficient compensation compared to the conventional pre-fault compensation technique and the existing minimum energy compensation techniques.

CONTENTS

CHAPTER 1	INTRODUCTION	1
1.1.	Definition of power quality	1
1.2.	Importance of power quality	2
1.3.	Power quality disturbances and indices	5
1.3.1.	Sags	6
1.3.2.	Interruptions	6
1.3.3.	Swells	7
1.3.4.	Overvoltage	7
1.3.5.	Undervoltage	7
1.3.6.	Harmonics	7
1.3.7.	Notches.....	7
1.3.8.	Voltage fluctuations	8
1.3.9.	Transients	8
1.4.	CBEMA and ITI curves	11
1.5.	Power quality improvement technologies	13
1.5.1.	Uninterruptible Power Supply (UPS)	13
1.5.2.	Dynamic Voltage Restorer (DVR)	15
1.5.3.	Static transfer switches and fast transfer switches.....	20
1.6.	Why using the DVR.....	21
1.7.	DVR topologies	22
1.7.1.	Topologies with no energy storage.....	22
1.7.2.	Topologies with energy storage.....	23
1.8.	DVR control strategies	24

1.9.	Transformerless DVR for medium voltage networks.....	25
1.10.	Thesis outline.....	25
CHAPTER 2 9-LEVEL MLI BASED ON CASCADED HBRIDGE TOPOLOGY		27
2.1.	Multilevel concept	27
2.2.	Single-phase full-bridge (H-bridge) inverter.....	29
2.3.	Multilevel inverter based on cascaded H-bridge topology..	31
2.4.	Multilevel inverter switching techniques	35
2.5.	Simulation results of 9-level three-phase cascaded multilevel inverter with PSCPWM switching technique....	39
CHAPTER 3 TRANSFORMERLESS DVR USING CASCADED MLI TOPOLOGY		43
3.1.	DVR compensation techniques	43
3.2.	System Configuration	43
3.3.	Pre-fault compensation technique.....	44
3.3.1.	DVR operation.....	45
3.3.2.	Simulation results	48
3.3.3.	Advantages and disadvantages of the pre-fault compensation technique	55
3.4.	Energy saving compensation technique (by Al-Hadidi)	55
3.4.1.	DVR operation.....	56
3.4.2.	Simulation results	59
3.4.3.	Advantages and disadvantages of the energy saving compensation technique (by Al-Hadidi)	74
3.5.	In-phase compensation technique.....	76

3.5.1.	DVR operation.....	76
3.5.2.	Advantages and disadvantages of the in-phase compensation technique	77
CHAPTER 4 THE PROPOSED MINIMUM ENERGY TRANSFORMERLESS DVR		
		79
4.1.	Introduction	79
4.2.	DVR control system.....	80
4.2.1.	Zero-power mode.....	80
4.2.2.	Minimum-power mode	84
4.3.	The proposed minimum energy compensation technique...	86
4.3.1.	Measurements	87
4.3.2.	Determination of the DVR operation mode	88
4.3.3.	Calculation of θ_{2opt}	89
4.3.4.	Generation of modulation signals.....	90
4.4.	System Configuration	92
4.5.	Simulation results	92
4.5.1.	Voltage regulation.....	93
4.5.2.	Sag compensation	94
4.5.3.	Swell compensation	115
4.5.4.	Flicker suppression	118
4.6.	Applying the proposed minimum energy transformerless DVR using capacitors as energy storage elements.....	120
4.7.	Comparison between the proposed minimum energy compensation technique and the other compensation methods.....	122

4.7.1.	Comparison between the proposed minimum energy compensation technique and the pre-fault compensation technique	123
4.7.2.	Comparison between the proposed minimum energy compensation technique and the energy saving compensation technique (by Al-Hadidi)	125
4.7.3.	Comparison between the proposed minimum energy compensation technique and the in-phase compensation technique	127
CHAPTER 5 CONCLUSIONS AND RECOMMENDATIONS		129
5.1.	Conclusions	129
5.2.	Future work	130
REFERENCES		131

LIST OF FIGURES

Figure 1.1	Ideal single-phase voltage waveform at 50 Hz. The peak value is 8.98 KV and the rms value is 6.35 KV.	2
Figure 1.2	An ideal three-phase voltage waveform at 50 Hz with a line-to-line voltage of 11KV rms. Shown are the line-to-neutral voltages of each phase.	2
Figure 1.3	The most significant waveform distortions associated with poor power quality.	9
Figure 1.4	ITI curve.	12
Figure 1.5	Configuration of online UPS.	14
Figure 1.6	Configuration of offline UPS.	15
Figure 1.7	General configuration of DVR.	16
Figure 1.8	DVR systems with various inverter topologies: (a) three-phase inverter, (b) three single phase full bridge inverter (6-leg inverter), (c) Cascaded H-bridge MLI.	18
Figure 1.9	Preferred/alternate configuration of a static switch.	20
Figure 1.10	DVR topology system 1.	23
Figure 1.11	DVR topology system 2.	23
Figure 1.12	DVR topology system 3.	24
Figure 1.13	DVR topology system 4.	24
Figure 2.1	Multilevel concept: (a) 3-level inverter, (b) generalized n-level inverter.	27
Figure 2.2	Generalized stepped waveform for n-level inverter.	28
Figure 2.3	Basic structure of single-phase full-bridge (H-bridge) inverter unit.	29
Figure 2.4	Waveforms of the switching signals and the corresponding output voltage of a 3-level inverter.	30
Figure 2.5	Four cascaded H-bridges with four separate dc sources.	32
Figure 2.6	Nine-level output phase voltage waveform.	33
Figure 2.7	Waveforms of PWM switching techniques: (a) Alternative Phase Opposition Disposition PWM (APOD), (b) Phase Opposition Disposition PWM (POD), (c) Phase Disposition PWM (PD), (d) Phase Shifted	38

	Carrier PWM (PSCPWM).	
Figure 2.8	Inverter system configuration.	40
Figure 2.9	PSCPWM switching control system.	41
Figure 2.10	Waveforms of the output voltages and currents.	42
Figure 3.1	DVR system configuration.	44
Figure 3.2	Phasor diagram of the pre-fault compensation technique.	45
Figure 3.3	Cases of voltage disturbances: (a) $ \vec{V}_1 $ lies to the left of line XX, DVR injects active power, (b) $ \vec{V}_1 $ lies to the right of line XX, DVR absorbs active power.	47
Figure 3.4	Generation of modulation signals.	49
Figure 3.5	The three-phase pre-fault voltages	49
Figure 3.6	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in case of a three-phase sag of 17.4% for 0.2 sec.	50
Figure 3.7	rms pu voltage of phase 'a' at the source-side and load-side in case of a three-phase sag of 17.4% for 0.2 sec.	51
Figure 3.8	Active and reactive power of source, load and DVR in case of a three-phase sag of 17.4% for 0.2 sec.	52
Figure 3.9	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in case of a 50.6% sag in phase 'a' for 0.2 sec.	53
Figure 3.10	rms pu voltage of phase 'a' at the source-side and load-side in case of a 50.6% sag in phase 'a' for 0.2 sec.	54
Figure 3.11	Active and reactive power injection from the DVR into the system in case of a 50.6% sag in phase 'a' for 0.2 sec.	54
Figure 3.12	Phasor diagram of Al-Hadidi's compensation technique.	56
Figure 3.13	Generation of the three check_one signals.	60
Figure 3.14	Generation of δ for the three phases	61
Figure 3.15	Generation of α for the three phases	61
Figure 3.16	Generation of V_{dvr} for the three phases.	62
Figure 3.17	Generation of modulation signals.	62
Figure 3.18	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in	63

	case of three-phase 17.4% sag for 0.2 sec.	
Figure 3.19	rms pu voltage of phase 'a' at source-side and load-side in case of three-phase 17.4% sag for 0.2 sec.	64
Figure 3.20	<i>check_one</i> signals in case of three-phase 17.4% sag for 0.2 sec.	64
Figure 3.21	DVR active and reactive powers in case of three-phase 17.4% sag for 0.2 sec.	64
Figure 3.21	DVR active and reactive powers in case of three-phase 17.4% sag for 0.2 sec.	65
Figure 3.22	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in case of three-phase 50.6% sag for 0.2 sec.	66
Figure 3.23	rms pu voltage of phase 'a' at source-side and load-side in case of three-phase 50.6% sag for 0.2 sec.	67
Figure 3.24	<i>check_one</i> signal in case of three-phase 50.6% sag for 0.2 sec.	67
Figure 3.25	DVR active and reactive powers in case of three-phase 50.6% sag for 0.2 sec.	68
Figure 3.26	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in case of single-phase 17.4% sag in phase 'a' for 0.2 sec.	69
Figure 3.27	rms pu voltage of phase 'a' at source-side and load-side in case of single-phase 17.4% sag in phase 'a' for 0.2 sec.	70
Figure 3.28	<i>check_one</i> signal in case of single-phase 17.4% sag in phase 'a' for 0.2 sec.	70
Figure 3.29	DVR active and reactive powers in case of single-phase 17.4% sag in phase 'a' for 0.2 sec.	71
Figure 3.30	Three-phase waveforms of source-side voltage, DVR injected voltage, load-side voltage and load current in case of single-phase 50.6% sag in phase 'a' for 0.2 sec.	72
Figure 3.31	rms pu voltage of phase 'a' at source-side and load-side in case of single-phase 50.6% sag in phase 'a' for 0.2 sec.	73
Figure 3.32	<i>check_one</i> signal in case of single-phase 50.6% sag in phase 'a' for 0.2 sec.	73