
**AIN SHAMS UNIVERSITY**
**FACULTY OF ENGINEERING**
ELECTRONICS AND COMMUNICATIONS DEPARTMENT

# EXTRACTION & MODELING FOR MULTIGATE TRANSISTOR PARASITICS

## A Thesis

Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

**Submitted By:**

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**Ain Shams University - 2008**

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Thesis: **Extraction & Modeling for Multigate transistor Parasitics**
Degree: **Master of Science in Electrical Engineering**

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# STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

The work included in the thesis was carried out by the author at the Engineering Physics and Mathematics Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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# CURRICULUM VITAE

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# ABSTRACT

Thesis Title: **"Extraction & Modeling for Multigate Transistor Parasitics"**

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In VLSI applications, the parasitic capacitance between signal lines can deplete our whole design. At low frequencies, parasitic capacitance is usually ignored, but in high frequency circuits, it can be a major problem. For example, in amplifier circuits with extended frequency response, parasitic capacitance between the output and the input can act as a feedback path, causing the circuit to oscillate at high frequencies. These unwanted oscillations are called parasitic oscillations.

The parasitic capacitance arises from an electrical coupling between one signal line and another signal line or a signal line and the substrate. In some designs, it becomes mandatory for us to reduce the parasitic capacitance of a particular electrical path with respect to other signals.

In this thesis, we introduce numerical simulations of this parasitic capacitance and the effect of changing different geometrical parameters of the FinFET transistor on parasitic capacitance. Numerical simulations takes a long time, hence they are not suitable for VLSI design due to the large number of transistors that exists within the design. Hence, the introduction of a compact model becomes a necessity. The starting models used in this thesis needed adjustments to properly model multi-fin FinFET transistors.

We verify the accuracy of the model by performing 3D numerical simulations using Calibre® xACT 3D, then performing parameter extraction and fitting. The structures used are triple-gate FinFETs, with the technology file being that of a world-renowned fab in Taiwan. These modifications improved the accuracy of the compact model to reach 2%

**Key Words**: FinFETs, Parasitic Capacitance, Parameter Extraction, Modelling, Fringing Gate Capacitance.

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## Summary

The Thesis is divided into five chapters in addition to the lists of contents, tables, and list of tables, and a list of references.

**Chapter One**: We provide the summary, abstract, and motivation for the thesis, Along with introduction to the thesis. In the introduction, we provide an overview of the technology and evolution over the past 40 years, and the advancement of transistor nodes and the challenges of technology.

**Chapter Two:** We provide an overview of why we use small transistor along with the roadblocks that the technology faces in term of device characteristics. Then we provide a quick introduction on multigate devices and their advantages. A Section about state of the art parasitic capacitance models is introduced.

**Chapter 3:** We provide an overview over the different algorithms for parasitic capacitance simulators. Then we describe the used simulator (Calibre® xACT 3D), along with its different input parameters.

**Chapter 4:** In this chapter, we provide an overview of the shape and parameters of the FinFET transistor used in the simulations. Then the compact model is ran against the simulations and the errors are measured, the errors are shown to be pretty high and hence we follow with the analysis of the model parameters, coming up with the shortcoming of the model we are able to introduce modifications to the model.

**Chapter 5:** We show the results of the new model were compared with the simulations and then error analysis ensues and it is shown to be below 2%.

## Supervisors:

- Prof. Dr. Wael Fikry Farouk
- Prof. Dr. Mohamed Dessouky

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*"You are always a student, never a master. You have to keep moving forward." Conrad Hall*

*"You can't depend on your eyes when your imagination is out of focus."Mark Twain*

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