AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Design of energy efficient embedded SRAM

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by

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Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2013

Supervised By

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Cairo, 2017

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Date: 21 / 10 / 2017

Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electronics Engineering and Electrical Communications, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Faculty of Engineering – Ain Shams University
Electronics and Communication Engineering Department

Thesis title: **"Design of energy efficient embedded SRAM"**
Submitted by: **Mostafa Fouad Farid Abdelhady Helmy**
Degree: **Master of Science in Electrical Engineering**

Abstract

VLSI circuits continue to explore new areas of contribution in different applications. The CMOS scaling helps in enhancing the spread of VLSI circuits. One of these applications is low-voltage circuits. Low voltage circuits use very low supply voltage to decrease both active and leakage energy. Memories systems, especially SRAMs which spread widely in different applications, will benefit a lot from low-voltage operation.

Consequently, low-voltage operation SRAM memories are attractive. Moreover, they open a new area of contribution. The area of energy constrained applications, which has a lower performance requirements but aggressive energy requirements. So, SRAM that offers read and write functionality at the lowest possible supply voltage will give a great opportunities in this application domain.

This work explores the design of SRAM system blocks able to work within temperature range -40 to 125. Process corners and Monte Carlo analysis are used for further verification of these blocks and their margins. Furthermore, the limit of low-voltage operation for traditional SRAM and periphery circuits. Moreover, additional circuits as Read and Write assist techniques circuits are implemented to reach a low voltage operation with a normal 6T bitcell. The applied technique gives a great saving in energy compared to other conventional techniques. Also, a timing technique used to overcome assist associated halfselect problem. A test macro of 8-Kbit is designed in 65nm CMOS technology. Simulations show that the design is capable of working down to 0.5V with access time

of 1.77ns in nominal condition and 339ns in low-voltage conditions. The macro is tested on different process corners at both voltage conditions.

In addition to macro design, level shifters for interfacing with memory are also implemented with a new technique extending the conversion range of nominal level shifters by 200mV across the same temperature range. Lastly a test chip is implemented for testing purposes with area of 4mm^2 packing a memory of 0.9Mbits. Different implementations of the 8-kbit macro are packed helping a fully characterization and testing.

Keywords: SRAM, Low-voltage, Memories, Level shifter, Assist technique.

Thesis Summary

Energy source limited applications have more functions been added to them across years. In hand held devices as watches, observing the change from simple applications as displaying time to a complicated applications as internet surfing is a good example. As this increase in functionality appears in hand held devices it also reaches more energy restricted application as biomedical ones.

Increasing functionality on a chip will consequently increase the need of a large memory consuming large energy and area and restricting the lifespan of the application.

Limiting the energy dissipated by CMOS logic in these chips can be achieved by decreasing the supply voltage, while SRAM memory is restricted in this reduction due to its failure in operation under low voltage.

Therefore this thesis aims to design SRAM memory able to work under lowest possible voltage, moving through each design phase schematic, physical and chip level using UMC 65nm technology. The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references and one appendix.

Chapter 1

In this chapter, there is pointing to the challenges and the main contributions of the thesis.

Chapter 2

This chapter introduces some CMOS device concepts, Memory background and state of art literature review on low voltage memories.

Chapter 3

Moving on to chapter three designing a full functional memory is achieved. In which the introduction of each block, giving its literature review, trade offs and simulation results for used design on the UMC 65nm technology, is stated.

Chapter 4

Reaching this chapter, enhancing the memory for low voltage application is presented. Where the enhance starts by testing the circuits at low voltage. Then, proposing new write and read assist technique. Lastly, proposing new level shifter to enhance communications. Verification is done on each circuit using corner simulation and Monte Carlo analysis.

Chapter 5

System simulation and characterization are introduced in nominal and low voltage in this chapter. Also, physical implementation are shown moving from block level to Chip level verifying the design ,in all levels, physical and functionality wise.

Chapter 6

This chapter ends the thesis by conclusions and future work that can be done.

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