Ain Shams University

Faculty of Engineering

Computer and Systems Engineering Department

Reconfigurable Media Processor for Augmented Reality Applications

A Thesis

Submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

Submitted by

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Degree : **Master of Science in Electrical Engineering (Computer and Systems)**

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Computer and Systems Engineering).

The work included in this thesis was carried out by the author at the Computer and Systems Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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Real time processing of image and video applications, especially *Augmented Reality (AR)* systems is a demand in many computer vision applications, e.g. video surveillance, traffic management and medical imaging. *Augmented Reality (AR)* is divided into vision processing engine and graphics processing engine. Those two processing engines use highly computational intensive tasks such as image segmentation, object recognition, and feature tracking. The processing of those functions requires high computational power, especially when they are applied on *high-definition (HD)* input video frames. The processing of video and image algorithms of real time AR is not capable of running on devices efficiently with low computing power at a reasonable frame rate. The collaboration of the *CPU* and hardware accelerators provides an efficient solution for this problem.

In this thesis, the presented approach targets offloading highly computational pixel processing modules from *processing system (PS)* to *programmable logic (PL)* taking the advantage of *High Level Synthesis (HLS)* tool flow to accelerate the implementation of compute-intensive pixel processing tasks of AR. Hardware accelerators for AR processing tasks are proposed. The accelerators are applied on full HD video input stream at 1080p60 of HDMI input. The performance improvement through hardware acceleration decreases the CPU utilization and increases the frame rate.

Keywords: Augmented Reality (AR), Computer Vision (CV), High Level Synthesis (HLS), ZYNQ, Field Programmable Gate Arrays (FPGAs).

SUMMARY

This thesis demonstrates the advantage of implementing the computational intensive tasks of AR video and image processing tasks as hardware accelerators using HLS.

The thesis is in seven chapters organized as follows:

Chapter One begins with an overview of the real time challenge of the AR systems, the motivation behind this dissertation, the scope and objectives of our work, and the outline of chapters.

Chapter Two, A brief introduction to AR is presented. It demonstrates AR different types, AR architecture, and the related work. The advantage of markerless-based AR over marker-based AR is discussed.

Chapter Three, Embedded AR is illustrated with a survey on the previous work and its architecture. A comparison between different embedded approaches for AR is presented. In addition, a brief introduction to HLS with its constraints, optimization techniques on FPGA and advantage compared to HDL is given.

Chapter Four, the infrastructure of *ZYNQ* platform, its architecture, capabilities and restrictions for the implementation of AR architecture is presented. A quick overview about the used *target reference design (TRD)*, and the Linux operating system for the application (*PetaLinux*) are given.

Chapter Five is divided in two sections. First, the software and the hardware implementation of canny edge detection are presented. In the other section, the software and hardware implementation of feature detection and extraction for markerless AR are presented. We use *OpenCV* libraries and *HLS* video libraries.

Chapter Six, the evaluation and experimental results of the implemented hardware accelerators are presented. This chapter is divided into three sections. First the results of those hardware accelerators using Vivado *HLS* simulation are illustrated. Second, the optimization directive results are presented to show the impact of optimization directives on area and performance. Finally, the profiling results of the hardware accelerators on ZYNQ platform are presented.

Finally, the thesis ends by extracting conclusions and future work that will be done based on this work.

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