AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications Engineering Department

Clock and Data Recovery Circuits for High-Speed Serial-Links

A Thesis

Submitted in Partial Fulfillment of the Requirements for the

Degree of Master of Science in Electrical Engineering

By

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B.Sc. in Electrical Engineering

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Ain Shams University, 2011

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

﴿ وَقُل رَّبِّ زِدْنِي عِلْمًا ﴾

صَدَقَ اللَّهُ العَظِيم

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Statement

This thesis is submitted to the department of Electronics and Communications Engineering, Faculty of Engineering, Ain Shams University, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Ahmed ElSayed Mohammed AbdelRahman, "Clock and Data Recovery Circuits for High-Speed Serial-Links," M.Sc. dissertation, Ain Shams University, Cairo, Egypt, Dec. 2017.

This thesis presents system and circuit design techniques for fast-locking all-digital phase-interpolator (PI)-based clock and data recovery (CDR) circuits. The target application is burst-mode (BM) communication systems such as passive optical networks (PONs), memory interfaces and energy proportional serial-links with multi-channel operation in deep sub-micron CMOS technologies.

The objective of this thesis is driven by the need for fast-locking CDR architectures that can be used for BM transmission without sacrificing the jitter performance — a trade-off commonly encountered in the design of BM-CDR circuits. The proposed technique allows closed-loop PI-based CDR circuits to meet the ultra-short locking time requirements set by BM communication systems. The main advantage of the proposed technique is maintaining superior jitter performance by the feedback action in contrast to common open-loop architectures.

On the system level, a new phase search technique that improves the locking speed of conventional (PI)-based CDR circuits is proposed. This technique employs successive approximation register (SAR) algorithm that achieves fast phase locking through binary phase search, instead of following the typical phase tracking trajectories of closed-loop feedback systems. The SAR algorithm is activated at startup or at the beginning of new data bursts to achieve phase lock in few tens of bit-periods. Once lock is achieved, the SAR algorithm is deactivated and the result is passed to a digital loop filter (DLF) of a conventional PI-based CDR to carry out further phase tracking and maintain the required jitter performance.

On the circuit level, the relatively short delay of the CDR loop encompassing the SAR algorithm (SAR-CDR) is exploited to achieve further improvements in the locking speed by operating its constituent blocks at a higher system frequency. This frequency is independent of the main clock supplied to the rest of the system and is set to its maximum value according to the loop delay. This results in additional boost to the locking speed and allows PI-based CDRs to achieve phase lock in a tiny fraction of the time achieved by conventional designs. To reduce the total area, block reuse is employed by placing the SAR block in place of the most significant N-bits of the Accumulator (ACC) feedback register. This is achieved by modifying the conventional design of the SAR unit.

To demonstrate the effectiveness of the proposed phase locking technique, a 10 Gbps half-rate all-digital PI-based CDR circuit that targets the stringent SONET OC-192 jitter specifications is analyzed and designed. A top-down design methodology is adopted throughout this work for implementing the proposed CDR circuit in a standard 65 nm low-power CMOS technology with 1.2 V supply. The design process begins by developing a linearized frequency-domain model to optimize the system parameters and extract the different blocks requirements for the targeted system specifications. Moreover, system functionality and performance are verified using time-domain behavioral models built with MATLAB/Simulink and Verilog-A. Next, each block is designed, simulated and its performance is verified across process and temperature corners with post-layout simulations. Finally, the complete system is integrated and the performance improvements are verified and compared to the performance of state-of-the-art open-loop CDR architectures.

The implemented CDR employing the proposed technique shows 62.5–125-fold locking speed improvement by reducing the locking time from 800 ns to only 6.4–12.5 ns with ±60 ppm maximum tolerable frequency offset between the transmitter and the receiver. It consumes 8.2 mW from 1.2 V supply with an energy per bit FoM of less than 1 pJ/Bit while occupying an active area of $70\mu\text{m} \times 90\mu\text{m}$.

Key words: Clock and data recovery circuits for high-speed serial-links, wireline communication, burst-mode communication systems, bang-bang phase detector, successive approximation register, phase interpolator

Summary

This thesis is divided into five chapters.

Chapter 1 introduces the dissertation and discusses the motivation for this work, followed by the thesis outline.

Chapter 2 presents necessary background for the research presented in this thesis. It presents an overview on serial-links and BM communication systems and the main figures of merits (FoMs) for wireline transceivers. Moreover, it includes a literature review on conventional open-loop and closed-loop CDR architectures and highlights their main differences and respective advantages and disadvantages. Towards the end of this chapter, more emphasis is given to the all-digital implementation of PI-based CDR circuits.

Chapter 3 begins with a description of the proposed binary search technique used to improve the locking speed of PI-based CDR circuits. Then, detailed system analysis and design is given for conventional PI-based CDR circuits to meet the targeted system specifications using frequency-domain linear models. Towards its end, the proposed integration of the successive approximation algorithm inside a conventional PI-based CDR is given and the complete system is described and verified with time-domain behavioral simulations.

Chapter 4 discusses the circuit-level design of the main building blocks of a 10 Gbps CDR circuit implemented in standard 65 nm LP CMOS process technology. It includes schematics, layouts and simulation results for all the required blocks and also integration and verification results of the proposed CDR. It ends with a summary of the achieved performance improvements and a comparison to state-of-the-art open-loop architectures.

Chapter 5 concludes the work in this thesis and discusses the strengths and weaknesses of the proposed solution. It also provides suggestions for future improvements, optimizations or other features that can be added to the CDR.

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