A Novel Approach to Air Vehicle Autopilot Mission with Increased Reliability and Flexibility

By
Eng. Hany Mamdouh Mohamed Abd El-monaam

A Thesis Submitted to the
Faculty of Engineering at Cairo University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science

In

Electronics and Electrical Communications Engineering

Faculty of Engineering,
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Summary:

In this work, a novel strategy for a flexible FPGA implementation of autopilot is presented. The implementation improves the reliability by allowing redundant calculations. This is achieved through very high processing speed. The power is reduced due to minimization of hardware by employing time-sharing of resources. Control is made flexible by allowing the hardware to be driven through instructions provided externally by the user. As a case study, an autopilot for space application was chosen. This application needs a high grade of reliability and also flexibility. The proposed FPGA design is firstly implemented in a high level of abstraction, using the VHDL language. Then a hardware implementation using FPGA

(XILINX SPARTAN 3AN) is performed. A useful comparison between the CPU-based approach for autopilot and the proposed FPGA is performed using real data acquired through hardware in the loop (HIL) experiment.

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Abstract

In this work, a novel strategy for a flexible FPGA implementation of autopilot is presented. The implementation improves the reliability by allowing redundant calculations. This is achieved through very high processing speed. The power is reduced due to minimization of hardware by employing time-sharing of resources. Control is made flexible by allowing the hardware to be driven through instructions provided externally by the user. As a case study, an autopilot for space application was chosen. This application needs a high grade of reliability and also flexibility. The proposed FPGA design is firstly implemented in a high level of abstraction, using the VHDL language. Then a hardware implementation using FPGA (XILINX SPARTAN 3AN) is performed. A useful comparison between the CPU-based implementation for autopilot and the proposed FPGA is performed using real data acquired through hardware in the loop (HIL) experiment.

The performance of the proposed FPGA autopilot design can be measured by two criteria: processing time and accuracy. The calculation of the four channels $б_1$, $б_2, б_3$ and $б_4$ takes 128 cycles in sequence with 10.935 ns (91.45MHz) each, so the total processing time will be 1.4 us. Meanwhile for the SBC (Single Board Computer) case with clock 800 MHz based on MS-DOS 6.22 operating system, it takes about 20 us. Based on this calculation, a least median squared method is used to compute error of the output command of AP (Autopilot) which is found 2.58, 1.07, 2.09, and 0.65 in minutes. These values are acceptable for the dynamics of autopilot for the proposed air vehicle.

A case study is presented to quantify the potential gain of using the excess processing capacity to improve reliability. The study shows that readings from multiple sensors can significantly improve performance. However, using more than three sensors is not significant valuable.

Chapter 1

Introduction

1.1 Introduction

Designing a real time embedded control system is a very critical issue for missiles requiring high flexibility and reliability. Military standard definition of reliability is the probability that an embedded system will perform a required function without failure under stated conditions for a stated period of time.

The main reliability issue is that the embedded control system cannot safely be shut down for repair. Alternatively it may be too inaccessible to repair, especially for space systems. The traditional approach of designing and implementing a real time embedded control system is based on using either ordinary microprocessors (µP) or microcontrollers (µC), which have many more peripherals on chip.

The traditional design of AP is based on a PC/104+ single board computer (SBC) [1]. It is based on x86 architecture using MS-DOS operating system. This approach has a lot of overhead and is not very reliable. In case of using SBCs, an operating system is required, which should be a real time operating system (RTOS) [2]. This opens the implementation to bugs and imposes significant overhead. Hence getting a reliable solution based on SBC will be very expensive.

Our research target is the design and implementation of a classical Autopilot-PID controller of the embedded control system for missile using FPGA hardware. The novelty of this work is based on a reconfigurable FPGA hardware design and implementation for the autopilot [3].

The flexibility of an FPGA provides a unique benefit for performing sensor simulation. As requirements change and components are added or removed, the FPGA controller can be reconfigured for these changes without significant hardware rework. You can change the processing functionality of the FPGA by making changes to the software.

FPGAs offer a middle point between application-specific integrated circuits (ASICs) and central processing units (CPUs). ASICs have the lowest power consumption but also the lowest flexibility: they can be used for only one purpose. FPGAs, on the other hand, typically exhibit at least an order of magnitude more power consumption than ASICs, but they also provide greater flexibility: they can be programmed and reprogrammed.

Furthermore, the re-programmability of the FPGA also makes it an ideal choice for hardware that needs to be upgraded or modified often [3]. Currently, the benefits that FPGAs offer come at a price. While CPUs are simple to program and languages made to program CPUs are generally high-level and easy to learn, those specially trained to use the tools and languages developed specifically for designing digital circuits can only program ASICs and FPGAs.

FPGA designers typically use a hardware description language (HDL) such as VHDL or Verilog to define the behavior of the FPGA. Although recent developments have raised the level of abstraction by allowing HDL designs to be constructed from programs written in C, the barrier of entry can be reduced even more by enabling software engineers to start at an even higher level of abstraction and program FPGAs in a paradigm familiar to many object-oriented programming.

In the introduced thesis, the task of AP is considered as a case study. The internal resources of the FPGA are configured according to the structure of the autopilot. The proposed configurable FPGA solution is considered cheap and has the parallel nature of hardware implementation. The processing time of the proposed FPGA autopilot design is faster than SBC even with higher SBC clock due to the overheads of the SBC is performing [1]. The power consumption and compactness of the FPGA solution is more suitable than SBC.