



بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ



شبكة المعلومات الجامعية التوثيق الالكتروني والميكروفيلم



شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكرو فيلم

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Design of Analog VLSI Supervised-Learnable Neural Cell

by

Rany Amir Tawfik Gad El-Sayed

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE
in
COMPUTER ENGINEERING

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GIZA, EGYPT

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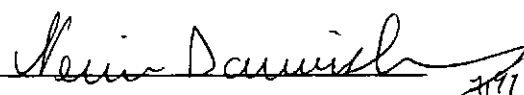
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LIST OF ABBREVIATIONS

w	synapse weight
E	error in backpropagation rule
δ	local gradient
β	Conductance coefficient
C_L	Storage capacitance
C_{ol}	Gate-drain overlap capacitance
C_{ox}	Gate capacitance (excluding overlap capacitance)
C'_{ox}	Gate capacitance per unit area
G	Channel conductance
L	Effective channel length ($L_{drawn}-2L_D$)
L_D	Lateral diffusion distance
N_{sub}	Substrate doping
R_s	Source resistance of the signal voltage source
t_{ox}	Gate-oxide thickness
U	Gate voltage falling rate for switching MOS
V_G	Gate voltage
V_H	High value of V_G in switching MOS
V_L	Low value of V_G in switching MOS
V_s	Signal voltage at the source
V_T	Threshold voltage with back-gate bias
V_{To}	Zero-bias threshold voltage
$v_d(t)$	Error voltage at drain end at time t
v_{dn}	Error voltage at drain end after gate voltage reaches V_L
v_{dm}	Absolute value of v_{dn}
W	Channel width
n	a constant between 1 and 2
V_t	is the thermal voltage= KT/q , where K is Boltzmann's constant, T is the device temperature in degrees Kelvin, and q is the charge of an electron
I_{Do}	is the effective drain current in the subthreshold operation