

## AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING

Computer and Systems Engineering Department

# Implementation and Optimization of Video Coding Techniques

#### **Thesis**

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## **English Approval sheet**

### **STATEMENT**

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Computer and Systems Engineering).

The work included in this thesis was carried out by the author at the Software Engineering Competence Center (SECC), Information Technology Industry Development Agency (ITIDA), Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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### **ABSTRACT**

With the multimedia revolution in full swing and with the continuously-emerging multimedia codecs and formats, portable multimedia players have become one of the most popular electronic devices. Some players support a single codec and receive its input in a single way like DVD players. Designing a portable multimedia player that supports several codecs encloses many design issues and challenges. The main challenge is optimizing the decoding process for enhancing the player performance, especially for the latest coding standard H.264.

Many approaches for the implementation and optimization of H.264 Baseline profile decoder have been developed in previous researches. In addition, several enhancement and speedup techniques for improving the H.264 deblocking filter performance have been developed in the literature.

In this research, a new parallelization approach for video player on an embedded asymmetric dual-core architecture with the two cores having significantly different performances was proposed, the player supports H.264 Baseline profile and Xvid video files. In addition, several enhancement and optimization techniques were presented at the system level and code level. It was proven through a performance comparison using many test samples that the implemented video player with the proposed parallelization approach and optimization techniques has a significant performance improvement versus previous implementations in the literature survey.

H.264 deblocking filter is one of the most powerful tools in H.264 decoding software that is used to improve the visual quality of decoded frames by removing the blocking artifacts; however it increases the computational complexity of the H.264. Two categories of enhancement and speedup techniques were proposed: standard-compliant techniques improving the deblocking performance by reducing the computation complexity, and standard-noncompliant techniques which propose some modifications on the original deblocking filter algorithm for further improvement of

the performance with tiny quality degradation. The proposed enhancement techniques showed significant performance improvement with tiny quality degradation, especially for videos encoded in low-bit rates.

Keywords: embedded system, video player, video coding, H.264, Xvid, dual-core architecture, parallelization, Deblocking filter, Optimization, Performance improvement

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## LIST OF ABBREVIATIONS

2 CDD	2 d Consulta Dada all'a Data
3GPP	3rd Generation Partnership Project
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
AVC	Advanced Video Coding
BIOS	Basic Input/Output System
BS	Boundary Strength
CAVLC	Context-Adaptive Variable Length Coding
CE	Codec Engine
CIF	Common Intermediate Format (352 × 288 resolution)
CMEM	Codec Memory
CODEC	enCOder / DECoder pair
DEM	Data Exchange Mechanism
DMA	Direct Memory Access
DSP	Digital Signal Processor
DVB-H	Digital Video Broadcasting-Handheld
DVD	Digital Versatile Disc
FFmpeg	Fast Forward MPEG
GPL	General Public License
IDCT	Inverse Discrete Cosine Transform
IEC	International Electrotechnical Commission
IMS	IP Multimedia Subsystem
IQ	Inverse Quantization
I-slice	Intra Slice
ISO	International Organization for Standardization
ITU-T	International Telecommunication Union Telecommunication Sector
LGPL	Lesser/Library General Public License
JVT	Joint Video Team
LF	Loop Filter
LOP	Line Of Pixels
MB	MacroBlock
MC	Motion Compensation
MMS	Multimedia Messaging Service
MMU	memory management unit
MPE	Media Processing Engine
MPEG	Moving Picture Experts Group
MV	Motion Vector
NAL	Network Abstraction Layer
PAL	Phase Alternating Line

PE	Processing Element
PPE	Power Processor Element
P-slice	Predicted Slice
PSNR	Peak Signal to Noise Ratio
PSTN	Public Switched Telephone Network
QCIF	Quarter CIF (176 × 144 resolution)
QP	Quantizer Parameter
QVGA	Quarter Video Graphics Array (320 × 240 resolution)
RGB	Red-Green-Blue
RISC	Reduced Instruction Set Computer
SIMD	Single Instruction Multiple Data
SoC	System-on-Chip
SPE	Synergistic Processor Elements
SPI	Server Programming Interface
TCP/IP	Transmission Control Protocol / Internet Protocol
USB	Universal Serial Bus
VCEG	Visual Coding Experts Group
VCL	Video Coding Layer
VGA	Video Graphics Array
VLC	VideoLAN Client media player
VLD	Variable Length Decoder
VLIW	Very Long Instruction Word
VPSS	Video Processing Subsystem
xDM	eXpress Digital Media
YUV	Luminance/Chrominance color space
3GPP	3rd Generation Partnership Project
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
AVC	Advanced Video Coding
BIOS	Basic Input/Output System
BS	Boundary Strength
CAVLC	Context-Adaptive Variable Length Coding
CE	Codec Engine
CIF	Common Intermediate Format (352 × 288 resolution)
CMEM	Codec Memory
CODEC	enCOder / DECoder pair
DEM	Data Exchange Mechanism
DMA	Direct Memory Access
DSP	Digital Signal Processor
DVB-H	Digital Video Broadcasting-Handheld
DVD	Digital Versatile Disc
FFmpeg	Fast Forward MPEG
GPL	General Public License

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### Chapter 1

### INTRODUCTION

#### 1.1 **OVERVIEW**

Embedded multimedia applications became vital for almost all aspects of modern life. Designing an embedded video player requires the optimizing the decoding process for enhancing the player performance, especially for the latest coding standard H.264. Many approaches for the implementation and optimization of H.264 Baseline profile decoder have been developed in previous researches. In addition, several enhancement and speedup techniques for improving the H.264 deblocking filter performance have been developed in the literature.

In this thesis, we propose a video player parallelization and optimization approach for embedded asymmetric dual-core architecture along with implementation which proved to have significant performance improvement versus previous implementations.

For H.264 deblocking filter several enhancement techniques were proposed, which proved to achieve performance improvement with little quality degradation whilst subjective quality was maintained.

#### 1.2 GENERAL RESEARCH OBJECTIVE

With the multimedia revolution in full swing and with the continuously-emerging multimedia codecs and formats, portable multimedia players have become one of the most popular electronic devices. Designing a portable multimedia player that supports several codecs and receives its input from different sources like a USB flash or real-