AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Computer and Systems Engineering

IC Placement Automation Using Constraints

A Thesis submitted in partial fulfilment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

(Computer and Systems Engineering)

by

Sherif Mohamed Saif El-Deen Ibrahim Ali Moussa

Master of Science in Electrical Engineering

(Computer and Systems Engineering)

Faculty of Engineering, Ain Shams University, 2006

Supervised By

Prof. Salwa Mohamed Mahmoud Nassar

Prof. Hazem Mahmoud Abbas

Prof. Mohamed Amin Dessouky Prof.

Mohamed Watheq Ali El-Kharashi Cairo

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AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
CAIRO - EGYPT

Name: Sherif Mohamed Saif El-Deen Ibrahim Ali Moussa
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Examiners Committee

1. **Prof. Marie-Minerve Louërat** **(sent report by email. Prof. Mohamed Watheq Ali El-Kharashi on her behalf)**
   Professor at Université Pierre et Marie Curie,
   Paris 6, France. ……

2. **Prof. Hani Fikry Ragai**
   Professor at Electronics and Communications Engineering Dept.,
   Faculty of Engineering - Ain Shams University. ……

3. **Prof. Mohamed Amin Dessouky**
   Professor at Electronics and Communications Engineering Dept,
   Faculty of Engineering - Ain Shams University. ……

4. **Prof. Mohamed Watheq El Kharashi**
   Professor at Computer and Systems Engineering Dept.
   Faculty of Engineering - Ain shams University**.** ……

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Statement

This thesis is submitted as a partial fulfilment of Doctor of Philosophy in Electrical Engineering, Faculty of Engineering, Ain Shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Sherif Mohamed Saif El-Deen Ibrahim Ali Moussa

Signature

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Date: 29 July 2015

Researcher Data

Name	: Sherif M. Saif El-Deen Ibrahim Ali Moussa
Date of birth	: 23/03/1977
Place of birth	: El-Minia, A.R.E.
Last academic degree	: Master of Science
Field of specialization	: Computer and Systems
University issued the degree	: Ain Shams University
Date of issued degree	: 2006
Current job	: Software Development

Abstract

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Satisfiability Modulo Theories (SMT) is an area concerned with checking the satisfiability of logical formulas over one or more theories. SMT can be well-tuned to solve specific problems in Electronic Design Automation (EDA) and other fields. Analog placers are important applications in EDA that use physical constraints to automatically generate small sections of layout. The work presented in this research shows that SMT solvers can be used for the automation of analog placement given some physical constraints. The proposed tool reads constraints that are entered by the user and uses Microsoft Z3 SMT solver to find valid placement solutions for some given analog blocks with the provided constraints. The tool represents the constraints in terms of equations that can be understood by the solver. It feeds those equations to the solver and then reads its output and converts the output into coordinates that represent locations of analog blocks. Accordingly it generates multiple layouts that fulfill some given constraints. The proposed system gives the user the option to choose one of the feasible solutions through specifying an aspect ratio or by selecting the optimum solution from the Pareto front of the generated shape function. Afterwards this research shows the results after deploying the proposed system on a cloud computing environment in order to enhance the results by achieving parallelization on several nodes. The proposed system yielded layouts with a good ratio of compaction compared to other techniques. The results were competitive from a speed perspective as well, when the provided circuits contain few blocks and many constraints.

Thesis Summary

The increasing functional complexity of system-on-chips, the lack of design automation for analog circuits, and the difficulties in analog design continually increase the bottleneck of analog components in chip design. Automation of analog layout and analog placement has been a research interest since the late 1980s. Layout of analog Integrated Circuits (IC's) has been manually designed by experts. Analog placers use a variety of mostly hand-entered physical constraints for design rules, placement and certain analog-specific layout conventions to automatically generate small sections of layout. The placement and the routing of an analog circuit have a severe impact on the function and performance. Thus, layout constraints are defined to make sure that the circuit fulfills the performance specifications. The number and diversity of constraints imposed on an analog circuit prevent approaches used in the digital domain from being used for analog design. With advanced nodes, a layout that meets every physical constraint can still fail to meet the electrical requirements of the design. Designers are quick to recognize the appropriate physical constraints that lead to correct electrical behavior using their experience. They have the ability to rapidly evaluate multiple solutions and quickly discard those options whose physical implementations do not meet the electrical constraints assigned to them. Hence, the latest generation of analog placement tools has been designed to create a variety of alternative layouts from which designers can choose. This puts the designer back into the picture by presenting choices rather than assuming that the software has chosen the best layout. The designer can make the choice since layout decisions involve compromise.

Satisfiability Modulo Theories (SMT) is an approach that can be used for solving constraint satisfaction problems. SMT combines Boolean satisfiability with term-manipulating symbolic systems. Boolean satisfiability is concerned with determining whether a formula expressing a constraint has a solution. Microsoft Z3 SMT solver is used in this work to find feasible solutions for the given constraints. Hence, the constraints should be translated into equations that can be understood by the Z3 solver, and afterwards the Z3 solver output should be translated into coordinates that can be used by the analog placer.

Cloud computing has emerged due to the increasing demand of variable system requirements and the need for more computing power with

different specifications at different time zones. In this research we deploy the analog placement platform on a cloud computing environment.
The thesis is divided into seven chapters in addition to the lists of contents, tables and figures as well as list of references and one appendix.

Chapter 1
In this chapter the analog placement concept is introduced, and its implementation challenges are highlighted. Proliferation of methodologies for resolving constraints such as satisfiability modulo theories is mentioned. Emergence of cloud computing and high performance computing is linked to the mentioned topics. This chapter includes the thesis introduction and presents its outline.

Chapter 2
This chapter presents a literature survey of analog integrated circuits placement. In addition it explains the physical constraints of analog circuits and their types. It also shows the emerging rapid prototyping flow and the importance of using constraints in this flow.

Chapter 3
This chapter explains SAT and satisfiability modulo theories. It provides the mathematical background and the methodology used by a solver to approach any problem. It discusses complexity of problems versus their tractability and decidability and brings to attention how constraints resolution can be handled according to this perspective.

Chapter 4
This chapter demonstrates the design details of the proposed system. It also shows how the satisfiability modulo theories is exactly used to approach the analog integrated circuits' placement problem.

Chapter 5
This chapter elaborates on the cloud computing and shows the steps needed to exploit them in this research. The deployment of the proposed system on the cloud is presented.

Chapter 6
This chapter shows the results and compares them to other results that were published in the literature. It shows the timing analysis and the effect of using the cloud. It discusses the different aspects of this work.

Chapter 7

This chapter ends the thesis by conclusion, summary and future work.

Key words:
Analog Layout, Automation, Cloud Computing, Constraints, Integrated Circuits, Placement, Satisfiability Modulo Theories.

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