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FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

INTEGRATED POWER MANAGEMENT IN CMOS TECHNOLOGY

A Thesis

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Submitted by

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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Power management has had an ever increasing role in the present electronic industry.

Battery powered and handheld applications require power management techniques to extend the life of the battery and consequently the operation life of the device.

Most systems incorporate several voltage regulators to supply various subsystems and provide isolation among such subsystems.

This dissertation demonstrates the design of Low dropout (LDO) voltage regulator for enhancing current efficiency; this design includes the core of the LDO and its voltage reference.

Additionally, the dissertation demonstrates a Design Methodology for LDO core and its voltage reference.

Two main constraints were regarded through the whole work; full integration in CMOS and suitability for low voltage applications.

These constraints were considered in two aspects; circuit analysis and design.

The LDO regulator and its voltage reference were designed in 130nm CMOS technology.

The designed LDO is capable of producing a regulated output voltage of 1.3 V from a Li-Ion battery supply, with a dropout voltage of 200 mV while supplying a load current of 200 mA with 100pF on chip output capacitor allowing for greater power system integration for SoC applications.

Simulation results show that LDO with its reference achieves current efficiency of 71.78% and 99.95% for min and max load current respectively, its line and load regulation is 0.45mV/V and 2.9 mΩ respectively; the total current consumption is 19.6 μA from a 1.5v supply for light load.

Key words: Low Supply Bandgap Reference, Capacitor-free LDO regulator, current efficiency, quiescent current, and power supply rejection ratio.

SUMMARY

This dissertation demonstrates the design and simulation of new linear voltage regulator in CMOS technology.

This LDO regulator has some features:

- Enhanced Current efficiency.
- Enhanced PSRR at low frequency

The dissertation is divided into six chapters organized as follows:

Chapter One: I present an introduction to Power Management chips and its importance.

Chapter Two: We compare between the conventional linear and LDO regulators; the selected topology is LDO to avoid using of charge pump circuit which is used in the conventional linear regulator and avoid its switching noise.

It also classifies LDO's specifications into:

- Static Specifications.
- Dynamic Specification.
- High frequency Specifications.
- LDO Stability.

Then it describes the effect of each element's size on the performance and how to make proper design for LDO.

Chapter Three: I focus on the voltage reference which is used to provide stable dc bias voltage with limited current driving capabilities for the core of LDO.

This Chapter starts with its basic operation and describes CTAT and PTAT effect and how to get temperature stable output voltage then introduces historical overview of its architectures.

Also it describes the general operation of start-up circuits and classifies them into two categories:

- Continuous conduction start-up circuit.
- Non-continuous conduction start-up circuit.

Then it discusses its design parameters and the effect of each element size on its performance.

In the end, it introduces the general tradeoffs of voltage reference and its design methodology.

Chapter Four: It introduces a new technique for LDO core to enhance its current efficiency by varying the quiescent current with its load current and compares its simulation results with conventional one.

Chapter Five: We introduce proposed technique for the voltage reference to enhance its low frequency PSRR which is important to minimize the size of used filter between voltage reference and LDO core and compares its simulation results with conventional one.

Chapter Six: I present the simulation results for the proposed LDO with varying process, supply and temperature then compares them with other architectures.

Appendix A: Power Supply Rejection Ratio of Conventional LDO at low frequency is analyzed.

Appendix B: Power Supply Rejection Ratio of BandGap Reference at low frequency is analyzed.

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LIST OF ABBREVIATIONS

LDO	**:**	Low Drop-Out
CTAT	**:**	Complementary To Absolute Temperature
PTAT	**:**	Proportional To Absolute Temperature
PVT	**:**	Process ,Voltage and Temperature
PSRR	**:**	Power Supply Rejection Ratio
BGR	**:**	BandGap Reference
PMIC	**:**	Power Management IC
CDMA	**:**	Code Division Multiple Access
ESR	**:**	Equivalent Series Resistance
LNR	**:**	Line Regulation
LDR	**:**	Load Regulation
TC	**:**	Temperature Coefficient
RMS	**:**	Root Mean Square
OPAMP	**:**	Operational Amplifier
SOC	**:**	Silicon On Chip
RHP	**:**	Right-Hand Plane
LHP	**:**	Left-Hand Plane
UGF	**:**	Unity-Gain Frequency
BW	**:**	Bandwidth
GBW	**:**	Gain-Bandwidth
PM	**:**	Phase Margin
OLG	**:**	Open Loop Gain
PPM	**:**	Parts Per Million
VCVS	**:**	Voltage Controlled Voltage Source
SIP	**:**	System in Package
IEEE	**:**	Institute of electrical and electronics engineers