شبكة المعلومات الجامعية

بسم الله الرحمن الرحيم

شبكة المعلومـــات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكروفيلم

﴿ قـسـم ﴾

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأفلام قد اعدت دون آية تغيرات

يجب أن

تحفظ هذه الأفلام بعيداً عن الغبار

في درجة حرارة من 15 – 20 مئوية ورطوبة نسبية من 20-40 %

To be kept away from dust in dry cool place of
15 – 25c and relative humidity 20-40 %

بعض الوثائق الأصلية تالفة

بالرسالة صفحات

لم ترد بالأصـــل

NOVEL CMOS AND BICMOS ANALOG CIRCUITS AND SYSTEMS

A THESIS

BY

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ABSTRACT

The switched-current (SI) technique is a quite immature current-mode sampled-data processing technique. Further research and development has still to be done to make it competitive with today existing commercial techniques.
One of the objectives of this research is to investigate novel structures that are advantageous compared to existing structures in terms of performance and signal processing accuracy.

Proposed techniques to improve the switched-current (SI) memory cell performance are presented. The first technique is mainly aimed to eliminate the charge injection in S2I memory cell that due to biasing current. The second technique is aimed to reduce the error due to non-zero output-input conductance ratio in the S2I memory cell.

In this thesis the advantages of using BICMOS current memory cell are presented. As application of BICMOS current memory cell, a design procedure of a third order low pass elliptic filter is presented.

The techniques of programming Q and center frequency w_0 independently based on second generation switched-current technique are presented. The most important advantage of these techniques is that they do not use programming switches in the signal path.

A new approach to develop Field Programmable Analog Arrays (FPAAs) which is based on switched-current technique is presented. The Configurable Analog Cell (CAC) is based on switched-current integrator. This (CAC) is easily configured to perform basic functions such as amplifications, attenuation, inversion, summation and integration. These elementary operations may then be combined to obtain more complex signal processing, such as filtering and data conversion. The proposed FPAA architecture has many

advantages such as it does not use extra switches to achieve the conductivity between the cells. It also does not use any switches in the signal path to reconfigure the cell. The use of a standard digital CMOS process makes the FPAA an attractive choice to integrate with its digital counter part (FPGA) to create field programmable mixed signal array.

As an example for FPAA a 5^{th} order low pass ladder filter is presented.

To my parents, wife, and daughters Yasmin & Yomna,

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