SUCCESSIVE APPROXIMATION REGISTER WITH CONTINUOUS DIS-ASSEMBLY ALGORITHM (SAR-CD) AND CIRCUIT DESIGN FOR TIME-BASED ANALOG TO DIGITAL CONVERTERS (TADC)

by

Karim Osama Ragab Mahmoud

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

in

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Title of Thesis:
Successive Approximation register with Continuous Dis-assembly Algorithm (SAR-CD) and circuit design for Time-based Analog to Digital Converters (TADC)

Key Words:
Time to Digital Converter (TDC); Voltage to Time Converter (VTC); Analog to Digital Converter (ADC); Biomedical circuits

Summary:
This work proposes a novel algorithm for analog to digital conversion. The algorithm is a modified version of the successive approximation algorithm in which binary sub-weights of the input maximum are used to evaluate the corresponding digital words in a cyclic manner. The proposed algorithm moves the conditioning between the evaluated bits from the analog domain to the digital domain. In folded versions of the successive approximation ADC circuits, in which bits are evaluated in an iterative fashion, digital to analog converters may not be needed anymore. This major advantage promises for reduction in fabrication area and power consumption. A full mathematical proof for the algorithm is also introduced. A new circuit design is developed to utilize the algorithm benefits. Results show competent power and reduction with state-of-art designs.

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Abstract

ANAlog to Digital Converters(ADC) and Digital to Analog Converters(DAC) define the boundaries between the analog and digital blocks in every machine. Optimizing powerful data converters means that more analog blocks can be digitized. Digital blocks are much easier in design and manipulation. Also they provide robust performance against noise with less power consumption and fabrication area benefitting every new fabrication technology.

Many ADC architectures have been proposed to serve wide range of applications. Choosing the right ADC architecture is based on many factors such as sampling rate, power consumption, fabrication area, resolution, robustness towards Process, Voltage and Temperature (PVT) changes. Sigma-delta, flash, pipelined and Successive Approximation Register (SAR) present a wide range of architectures.

Time-based ADC (TADC) is a special category of ADCs in which part of the data converter is desired to be digital in nature. The conversion between an analog quantity and the corresponding digital representation is done in two steps. The first step is to convert the analog quantity from voltage amplitude change into time change. In the second step, the signal representation in time change is converted to the corresponding digital binary representation. Most of the conversion effort is done in the second step. As the job is now simplified by the first step, the second one is expected to be implemented by digital components.

This work proposes a novel algorithm for analog to digital conversion. The algorithm is a modified version of the successive approximation algorithm in which binary sub-weights of the input maximum are used to evaluate the corresponding digital words in a cyclic mannar. The proposed algorithm moves the conditioning between the evaluated bits from the analog domain to the digital domain. In folded versions of the successive approximation ADC circuits, in which bits are evaluated in an iterative fashion, digital to analog converters may not be needed anymore.

This major advantage promises for reduction in fabrication area and power consumption. A full mathematical proof of the algorithm is also introduced. A new circuit design is developed to utilize the algorithm benefits. Results show competent power and area reduction with state-of-art designs.

This work is arranged as follows: Chapter II presents a brief review to the main analog to digital conversion approaches and measures. Also, Time-based analog to digital conversion concepts and circuit architectures are presented in the same chapter. The proposed SAR-CD algorithm with derived proof is introduced in Chapter III. Chapter IV proposes two circuit design architectures using the new algorithm with detailed analysis with results . It also introduces calibration algorithm for the second circuit architecture to compete for the Process Voltage Temperature (PVT) changes.

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