**Ain Shams University**
**Faculty of Engineering**
Engineering Physics and Mathematics Department

# Modeling and Simulation of Nano Scale MOSFET

**A THESIS**

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Doctor of Philosophy in Engineering Physics

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# STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Doctor of philosophy in Engineering Physics.

The work included in the thesis was carried out by the author at the Engineering Physics and Mathematics Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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# ABSTRACT

***Mona Mohamed Amin El Sabbagh, "Modeling and Simulation of nanoscale MOSFETs" Doctor of Philosophy dissertation, Ain Shams University, 2010.***

The rapid progress of CMOS technology pushes the dimension of devices in the nano scale range where quantum effects start to become important. Reduced channel lengths change the transport from drift diffusion to ballistic where scattering is rare. DG MOSFET operating in the ballistic regime differs from the common behavior in different aspects. The reduced silicon thickness leads to energy quantization, structural and electrical confinement of carriers. Much work was done to model these effects and rigorous numerical simulations were obtained.

As numerical simulation is time consuming and not suitable for circuit simulation, we proposed in this thesis a compact model where most of the effects resulting from the reduced dimensions are taken into consideration. The model uses a single expression for current for all regions of operation including linear and saturation, subthreshold and high gate bias. This ensures current continuity. The model is adjusted to be valid over a wide range of silicon and oxide thickness. The model also is suitable for long and short channel by use of tunable equation. A compact equation for direct tunneling gate current is also proposed. This equation takes into account the energy quantization and wave penetration at the oxide interface. The strength of the model presented here is demonstrated by comparison with numerical simulations. In fact, the analytic model gives strong agreement with numerical simulations for both drain and gate current with and without the use of high K material.

**Key Words**: DG MOSFETs, ballistic current, reflection coefficient, gate tunneling.

# Summary

The rapid progress of CMOS technology leads to reduced dimension. This results in the appearance of different quantum and short channel effects. The reduced channel length results in the transport of electron near the ballistic limit. In this regime of operation, the drain current characteristics differs from that of drift diffusion transport. The transport is with velocity approaching thermal velocity due to the reduction or even the absence of scattering. The saturation of velocity occurs near the source side and not at the drain side as would be the case in long channel MOSFETs. The exact prediction of the nano-scale MOSFET is obtained from numerical simulation. Although numerical simulation is accurate, it is time consuming and not suitable for circuit simulators. Moreover, DG MOSFET models neglect gate tunneling current.

In this thesis, the author proposed a compact model based on flux treatment of drain current in the ballistic limit. This model includes drain-induced barrier lowering (DIBL), two dimension (2D) electrostatics and energy band splitting. A single expression for all regions of operation is proposed. The drain current model contains ten fitting parameters to make it valid over a wide range of gate oxide and silicon thickness. A compact equation for gate current calculation with three fitting parameters is also proposed. The model is validated over a wide range of gate oxide and silicon thickness by numerical simulations.

The thesis contains four chapters, conclusion and future work, references list, and one appendix and is organized as given below.

**Chapter 1**

This chapter gives a background on the structure of DG MOSFET and its advantages. Physical effects arising from the reduced silicon and gate oxide thickness are summarized. Direct tunneling gate current and its variation with

dimension is also presented. As the gate length decreases the transport turns to be ballistic. The physics of ballistic and quasi ballistic nano MOSFET is explained in detail in this chapter.

**Chapter 2**

In this chapter, different types of compact models of nanoscale MOSFETs are summarized. Some of these models treat the case of ballistic transport only and others includes scattering. All of them fail to include 2D electrostatics, Drain induced barrier lowering and band splitting. Moreover most models are not valid over a wide range of silicon and oxide thickness.

**Chapter 3**

In this chapter, we present the physically based proposed compact model. The model is based on flux approach with the introduction of energy band splitting and DIBL. A single expression succeeded to simulate all regions of operation by adjustment of ten fitting parameters. The model is adjusted for different silicon and gate oxide thickness. An empirical equation for velocity calculation is used. This equation takes into account the variation of injection velocity with bias and dimension. Direct tunneling gate current is also modeled with the band splitting and wave penetration at gate oxide interface.

**Chapter 4**

Evaluation of the proposed analytical model is presented in this Chapter**.** The drain and gate model is compared with numerical simulation from NANOMOS simulator for a wide range of silicon and oxide thickness. The results shows good match between the proposed model and numerical simulation with error less than 6% for saturation region and not exceeding 10% in the linear region. Gate current is also validated over several oxide and silicon thickness. The results of comparison show an error of less than 10%.

Different high K materials are compared. The model succeed to capture the behavior of high K material with an error less than 10% which equal to that projected by ITRS 2008 for the year 2015.

Finally, the **conclusion** of our work after its comparison with numerical simulation is presented. In addition, suggestions for future work for the completion of this work are given.

Only one **Appendix** is found at the end of the thesis where variation method for the solution of Schrödinger equation is explained.

# List of Symbols

| | |
|---|---|
| $C_{ox}$ | Oxide capacitance per unit area ($F/m^2$) |
| $C_{si}$ | Silicon capacitance per unit area ($F/m^2$) |
| $C_g$ | Gate capacitance per unit area ($F/m^2$) |
| D | Density of states$(eV.m)^{-1}$ |
| $E_C$, $E_V$ | Conduction and valence energy (eV) |
| $E_F$ | Fermi level energy (eV) |
| $E_n$ | Energy of the level number n (eV). |
| $E_{Top}$ | Energy at the top of source barrier (eV) |
| $F^+$ | Positive going flux |
| $F^-$ | Negative going flux |
| $f(E)$ | Fermi-Dirac distribution function |
| $g_v$ | Degeneracy factor. |
| $h$ | Planck's constant (J.s) |
| $I_{DS}$ | Drain current per unit width (A/m) |
| $k$ | Boltzman constant J/K |
| $L$ | Channel length (nm) |
| $\ell$ | Low field region length (nm) |
| $m_l$ | Effective mass in the longitudinal direction |
| $m_t$ | Effective mass in the transverse |

| | |
|---|---|
| | direction |
| $m_d$ | Density of states effective mass. |
| $m_c$ | Conductivity effective mass. |
| $N_A$ | Acceptor concentration ($m^{-3}$) |
| $N_D$ | Donor concentration ($m^{-3}$) |
| $r$ | Reflection coefficient |
| $t_{ox}$ | Gate oxide thickness (nm) |
| $t_{si}$ | Silicon insulator thickness (nm) |
| $V_{DS}$ | Drain-source potential difference (V) |
| $V_{GS}$ | Gate-source potential difference (V) |
| $v_{inj}$ | Injection velocity (m/s) |
| $v_{th}$ | Thermal velocity (m/s) |
| W | Channel width (nm) |
| Á$_n$ | Fermi integral of order n |
| $\rho$ | Space charge density ($C/m^3$) |
| l | Mean free path (nm) |
| ψ | Wave function |

# List of abbreviation

| | |
|---|---|
| DG | Double gate |
| EOT | Equivalent oxide thickness. |
| MOSFET | Metal oxide field effect transistor |
| SG | Single gate |
| UTB | Ultra thin body |
| 2D | Two dimensional |

**LIST OF FIGURES**