AL-AZHAR UNIVERSITY
FACULTY OF ENGINEERING
ELECTRICAL ENGINEERING DEPARTMENT

Multirate Digital Filters Based on FPGA and Its Applications

A Thesis
Submitted inPartialFulfillment of the
Requirements for the Degree of M.Sc. inElectrical Engineering

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ABSTRACT

Digital Signal Processing (DSP) is one of the fastestgrowing techniques in the electronics industry. It is used in a wide range of application fields such as, telecommunications, data communications, image enhancement and processing, video signals, digital TV broadcasting, and voice synthesis and recognition. Field Programmable Gate Array (FPGA) offers good solution for addressing the needsof high-performance DSP systems.

The focus of this thesis is on one of the basic DSP functions, namely filtering signals to remove unwanted frequency bands. Multirate Digital Filters (MDFs) are the main theme here. Theory and implementation of MDF, as a special class of digital filters, will be discussed.

Multirate digital filters represent a class of digital filters having a number of attractive features like, low requirements for the coefficient word lengths, significant saving in computation and storage requirements results in a significant reduction in its dynamic power consumption.

This thesis introduces an efficient FPGA realization of a multirate decimation filter with narrow pass-band and narrow transition band to reduce the frequency sample rate by factor of 64 for noise thermometer applications. The proposed multiratedecimation filter is composed of three stages; the first stage is a Cascaded Integrator Comb (CIC) decimation filter, the second stage is a two-coefficient Half-Band (HB) filter and the last stage is a sharper transition HB filter.

The frequency responses of individual stages as well as the overall filter response have been demonstrated with full simulation using MATLAB. The design and implementation of the proposedMDF on FPGA (XILINX Virtex XCV800 BG432-4), using VHSIC Hardware Description Language (VHDL), has been introduced. The implementation areas of the proposed filter stages are compared. Using CIC-HB technique saves 18% of the design area, compared to using six stages HB decimation filters.

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LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CD	Compact Disk
CDMA	Code Division Multiple Access
CIC	Cascaded Integrator Comb
CIN	Carry Input
CLB	Configurable Logic Block
CLK	Clock
CMOS	Complementary Metal-Oxide Semiconductor
COUT	Carry Output
CPU	Central Processing Unit
CT	Computed Tomography
DLL	Delay-Locked Loop
DSP	Digital Signal Processing
DVD	Digital Video Disk
EC	Clock Enable
FIR	Finite Impulse Response
FM	Frequency Masking
FPGA	Field Programmable Gate Array
GCLK	Global Clock
HB	Half-Band
IFIR	Interpolated FIR
IIR	Infinite Impulse Response
IOB	Input/output Block

ISE	Integrated Software Environment
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LC	Logic Cell
LPF	Low-Pass Filter
LUT	Look-Up Table
MATLAB	Matrix Laboratory
MDF	Multirate Digital Filter
MRI	Magnetic Resonance Imaging
PC	Personal Computer
PCI	Personal Computer Interface
RAM	Random Access Memory
RC	Synchronous Set
ROM	Read-Only Memory
SBSRAM	Synchronous Burst Static RAM
SP	Synchronous Reset
TDMA	Time Division Multiple Access
UniDAQ	Universal DSP Data Acquisition board
Vcco	Output source voltage
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VI	Virtual Instrumentation Programming Package
VLSI	Very Large Scale Integrated circuits
Vocoders	Voice recorders
WE	Write Enable

LIST OF SYMBOLS

a, b	Filter coefficients
B_{in}	Bit width of CIC filter input
B_{out}	Bit width of CIC filter output
D	Differential delay
f	Frequency variable
f_c	Cut-off frequency
f_s	Sampling frequency
f_{st}	Stop frequency
$h(nT_1)$	Anti-aliasing filter
$h(mT_2)$	Anti-imaging filter
$F(z)$, $G(z)$, $H(z)$, $I(z)$	Transfer function
$H(\omega)$	Frequency response
k	Sample index for input signal
L	Interpolation factor
m	Sample index for output signal
M	Decimation factor
N	Filter order
S	FIR filter numberof stages
T_1	Sampling interval of the original signal ($T = 1 / f_s$)
T_2	Sampling interval of the decimated/interpolated signal
$x(n)$, $x(kT_1)$	Input discrete-time signals
$y(n)$, $y(mT_2)$	Output discrete-time signals
$X(z)$, $Y(z)$	z-transform of discrete-time signals
β	Conjugate-complex pole pairs