



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Transmitter design for high speed serial links

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by

Mohamed Megahed Mabrouk
Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Alexandria University, 2013

Supervised By

Dr. Sameh Assem Ibrahim
Prof. Mohamed Rizk Mohamed Rizk
Prof. Mohamed El Dessouky

Cairo, 2017



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Thesis title: Transmitter design for high speed serial links

Degree: Masters of Science in Electrical Engineering

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Statement

This thesis is submitted as a partial fulfillment of Master of Science inElectricalEngineering,FacultyofEngineering,AinshamsUniver-
sity. The author carried out the work included in this thesis, and no
part of it has been submitted for a degree or a qualification at any
other scientificentity.

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Date: dd Month yyyy

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Abstract

**Faculty of Engineering – Ain Shams University
Electronics and Communication Engineering Department**

Thesis title: **"Transmitter design for high speed serial links"**

Submitted by: **Mohamed Megahed Mabrouk**

Degree: **Master of Science in Electrical Engineering**

Abstract

This thesis presents a multi-standard transmitter design for high speed serial link applications. The target of the design is to achieve a dissipate power less than 1.25 pJ/bit while realizing all the standards' requirements.

The choice of multi-standard design is driven by the needs of the industry. With the evolution of I/O market, the time-to-market has become a crucial aspect in the market. Developing an IP for each standard can be a setback for fabless companies to meet the needs of many customers. However, the presence of a single IP that answers the need for all customers can achieve the required can prove to be cost and time efficient.

The design of multi-standard transmitters can be challenging for many reasons. First the varying output swing poses challenges on using voltage mode drivers. On the other hand, using current mode drivers can increase the power to almost 4 times of the voltage mode power. Other challenges include the different width's of the input parallel words and different equalization configurations. A literature survey has been made to review the possible solutions that can be used to design the transmitter.

The standard requirements were carefully reviewed. The system requirements were derived from the standards' requirements. Then a system model has been implemented and simulated to validate its performance. The circuits were then implemented relying on some of the solutions from the literature survey and some innovative ideas. The

main idea of the design relied on an innovative approach for the voltage mode driver. Two prototypes were implemented, one on 65 nm, which suffered from minor setbacks regarding mid-range swing and power consumption. However, those problems were addressed and solved in the prototype on 28 nm technology. Simulation results shows that both prototypes realize all standards' requirements while consuming 1.4 pJ/bit and 0.9 pJ/bit for 65 nm and 28 nm prototypes respectively.

Thesis Summary

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This thesis presents a multi-standard transmitter design for high speed serial link applications. The target of the design is to achieve a dissipate power less than 1.25 pJ/bit while realizing all the standards' requirements.

The choice of multi-standard design is driven by the needs of the industry. With the evolution of I/O market, the time-to-market has become a crucial aspect in the market. Developing an IP for each standard can be a setback for fabless companies to meet the needs of many customers. However, the presence of a single IP that answers the need for all customers can achieve the required can prove to be cost and time efficient.

The design of multi-standard transmitters can be challenging for many reasons. First the varying output swing poses challenges on using voltage mode drivers. On the other hand, using current mode drivers can increase the power to almost 4 times of the voltage mode power. Other challenges include the different width's of the input parallel words and different equalization configurations. A literature survey has been made to review the possible solutions that can be used to design the transmitter.

The standard requirements were carefully reviewed. The system requirements were derived from the standards' requirements. Then a system model has been implemented and simulated to validate its performance. The circuits were then implemented relying on some of the solutions from the literature survey and some innovative ideas. The main idea of the design relied on an innovative approach for the voltage mode driver. Two prototypes were implemented, one on 65 nm, which suffered from minor setbacks regarding mid-range swing and power consumption. However, those problems were addressed and solved in the prototype on 28 nm technology. Simulation results shows that both prototypes realize all standards' requirements while consuming 1.4 pJ/bit and 0.9 pJ/bit for 65 nm and 28 nm prototypes respectively. The thesis is divided into six chapters as listed below:

Chapter 1

This chapter is an introduction to state the problem, the proposal and the thesis organization.

Chapter 2

This chapter contains the literature survey for various blocks of the transmitter with a special emphasis on multi-standard publications.

Chapter 3

This chapter defines the system requirements from the standards and presents a system model that has been developed using Verilog-A to propose a possible multi-standard solution.

Chapter 4

This chapter presents the aspects of the circuit design of the multi-standard transmitter with special focus on the driver design for the two designed transmitters.

Chapter 5

This chapter represents the simulation results, layout screenshots, postlayout simulations for the first transmitter and the simulation and corner simulation results for the second transmitter.

Chapter 6

This chapter interprets the simulation results and concludes the outcome of this work.

Key words:

SerDes, Multi-standard, multi-protocol, voltage-mode