AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communication Engineering Department

Analog Design Automation for Pipeline ADC

A Thesis
Submitted in partial fulfillment of the requirements of the degree of
Master of Science in Electrical Engineering

Submitted by
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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communication Engineering).

The work included in this thesis was carried out by the author, a technical leader in IBM, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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This thesis aims to use MATLAB in the analog design automation cycle of pipeline ADC, starting from system level till transistor level. A 10 bits pipeline ADC will be used as a case study. 1.5bit/stage architecture is used and the complete 10 bits pipeline ADC is modeled in MATLAB/SIMULINK with its non-idealities. The simulation results are compared between ideal and non-ideal models.

Challenges of simulating analog circuits in MATLAB are introduced and two solutions are proposed. S-Factor, a novel analog design automation technique is introduced to address highly non-linear analog circuits. Building circuit core simulator into MATLAB is the second solution. Folded cascode op-amp and latched comparator are two case studies presented to demonstrate the successfulness of the proposed solutions.

Equation based analog design automation technique is implemented into MATLAB. The transistor level analog design automation is based on BSIM3v3 model equations which are verified with SPICE and ELDO simulators. Circuit designer functions and optimization functions are built to help the analog designer in solving the analog circuits in the MATLAB environment.

The complete pipeline ADC ADA flow will start from the system level then stage level passing to circuit level and ending by transistor level. 10 bits pipeline ADC will be used as a case study in the verification of the complete ADA flow. Moreover, the implemented circuit schematics will be presented and design values for the used folded cascode op-amp will be shown. The simulation results for the 10 bits pipeline ADC will be demonstrated.

Keywords: *equation-based, analog design automation, matlab, pipeline ADC, matspice, s-factor, folded cascode op-amp, latched comparator,*

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