AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Department

Fractional Digital Multiplying Delay Locked Loop Frequency Synthesizers

A Thesis submitted in partial fulfillment of the requirements of

a Master of Science degree in Electrical Engineering

Electronics Engineering and Electrical Communications Department

by

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Bachelor of Science degree in Electrical Engineering

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Thesis title: **"Fractional Digital Multiplying Delay Locked Loop Frequency Synthesizers"**

Submitted by: **Muhammad Swilam Abdelhaleem Ahmed**

Degree: **Master of Science in Electrical Engineering**

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Muhammad Swilam Abdelhaleem Ahmed

Signature

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Date: 11/08/2015

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Abstract

Faculty of Engineering Ain Shams University
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Abstract

Highly digital clock generator architectures, commonly implemented using digital phase-locked loops (DPLLs), are evolving as the preferred means for synthesizing high frequency on-chip clocks. By obviating the need for a large loop filter capacitor and high performance charge-pump, DPLLs offer many advantages over classical charge-pump PLLs. Their main benefits include small area, reduced sensitivity to analog circuit imperfections, immunity to process, voltage, and temperature (PVT) variations,

and easier scalability to newer processes. Recently, Digital Multiplying Delay Locked Loop (DMDLL) showed superior performance over the DPLLs for the same building blocks. Unfortunately, DMDLL is still limited to Integer multiplication only of the reference frequency which limits its fields of application. To overcome this drawback of DMDLLs, this thesis introduces two possible solutions.

The first one is by using the regular integer DMDLL followed by a set of open loop fractional dividers. The proposed open loop fractional divider is used to eliminate the deterministic jitter caused by the conventional fractional dividers without additional calibration. The proposed divider utilizes a new voltage comparator based Digital-to-Time converter (DTC) as an adjustable delay circuit to control the edges of the output clock of the divider. The proposed DTC proves to be power efficient considering its resolution and the frequency of the output clock. Detailed analysis of non-idealities of the proposed architecture and its effect on the cancellation of the deterministic jitter are presented and verified by simulations. Simulation results show that for an input frequency of 5.325 GHz and output frequency of 1 GHz, the proposed divider achieves a 0.2 ps of time resolution using a 10-bits DTC while consuming 3.72 mW and 1.17 mW from 1.2 V and 0.9 V supply,for 130 nm and 65 nm CMOS technology nodes, respectively.

The second solution is by proposing a new calibration free Fractional Digital MDLL (FDMDLL) clock multiplier where the

integer DMDLL itself is converted into fractional one. The new fractional MDLL relies on using a digital-to-time converter (DTC) to align the edge of the reference clock to the oscillator output clock. Moreover, a power efficient frequency locked loop (FLL) is proposed as a part of FDMDLL. The proposed architecture is simulated using 130 nm CMOS technology node. The output frequency ranges from 2-3 GHz from a 64 MHz reference frequency, The simulated integrated rms jitter is 0.77 ps at an output frequency of 2.4 GHz. The FDMDLL consumes 2 mW from a 1.2 V supply, and has an effective area of 0.21 mm^2.

Thesis Summary

Summary

The thesis is divided into six chapters as listed below:

Chapter 1

In this chapter a brief introduction is presented about frequency synthesizers, and more particularly the fractional-N phase locked loops emphasizing its importance in many applications.

Chapter 2

chapter 2 discusses the MDLL architecture and its benefits, provides background information on DPLLs and previous approaches to MDLL tuning, and highlights their sensitivity to analog non-idealities.

Chapter 3

This chapter introduces the first technique to realize the clock fractional multiplications using MDLL. This will be based on using an integer MDLL followed by a set of new open loop fractional dividers that are based on voltage comparator based digital-to-time converter.

Chapter 4

This chapter proposes a more general technique for the clock fractional multiplications using MDLL. In this technique the MDLL itself becomes fractional. This is done by adding a small modification to the MDLL system and the output from the MDLL is directly a fractional multiples of the reference frequency.

Chapter 5

Chapter 5 explores the circuit design of the proposed fractional digital multiplying delay locked loop (FDMDLL). In addition, simulations results are introduced.

Chapter 6

Chapter 6 starts with a summary of thesis and then lists thesis contributions. Finally, the chapter and the thesis end with the discussion of suggestions for future research.

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