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FPGA Implementation of LMS Adaptive Filter

By

Eng. Mohamed Salah Mohamed

A Thesis Submitted to the

Faculty of Engineering Ain Shames University

In Partial Fulfillment of the

Requirement of the Degree of

MASTER OF SCIENCE

In

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List of Abbreviation

ASIC	Application of Specific Integrated Circuit
CLB	Configurable Logic Block
CPLD	Complex Programmable Logic Device
DA	Distributed Arithmetic
DKCM	Dynamic Constant Coefficient Multiplier
DSP	Digital Signal Processing
EDK	Embedded Development Kit
FPGA	Field Programmable Gate Array
FPLD	Field Programmable Logic Device
FPU	Floating-Point Unit
HDL	Hardware Description Language
I/O	Input/output
IP	Intellectual Property
IPIC	IP Interconnect
IPIF	IP Interface
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
KCM	Constant Coefficient Multiplier
LE	Logic Element
LMS	Least-Mean-Square
LUT	Look-up Table
MAC	Media Access Control
MIPS	Million Instructions per Second
MMI	Monolithic Memories Inc.
MMU	Memory Management Unit
OPB	On-chip Peripheral Bus
PAL	Programmable Array Logic
PLA	Programmable Logic Array
PLB	Processor Local Bus
PLD	Programmable Logic Device
PROM	Programmable Read Only Memory
RAM	Random Access Memory
RISC	Reduced Instruction Set Co
RLS	Recursive Least-Squares
ROM	Read Only Memory
RTL	Register Transfer Level
SoC	System-on-Chip
SRAM	Static Random Access Memory
TLB	Translation Look-aside Buffer
UART	Universal Asynchronous Receiver-Transmitter
VCM	Variable Coefficient Multiplier
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration

Table of Content

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Abstract

Filtering signals in real-time requires dedicated hardware to meet demanding time requirements. If the statistics of the signal are not known, then adaptive filtering algorithms can be implemented to estimate the signals statistics iteratively [1].

Modern field programmable gate arrays (FPGAs) include the resources needed to design efficient filtering structures. Furthermore, some manufacturers now include complete microprocessors within the FPGA fabric. This mix of hardware and embedded software on a single chip is ideal for fast filter structures with arithmetic intensive adaptive algorithms.

This thesis aims to combine efficient filter structures with optimized code to create a system-on-chip (SOC) solution for various adaptive filtering problems. Several different adaptive algorithms have been coded in VHDL as well as in MATLAB and C. The designs are evaluated in terms of speed, hardware resources, and power consumption.

System identification is one of the most interesting applications for adaptive filters, especially for the Least Mean Square algorithm, due to its strength and calculus simplicity. Based on the error signal, the filter's coefficients are updated and after certain conversion time filter's coefficients becomes almost exactly the unknown system' coefficients .System identification was mapped into a hardware description language, VHDL. The hardware was synthesized using FPGA (Xilinx Spartan3 3s200ft256 kit) with 50 MHz clock. Testing and verification procedures are described in details.

Introduction

One of the most popular adaptive algorithms available is gradient algorithm also called least-mean-square (LMS). Its popularity comes from the fact that it is very simple to be implemented. As a consequence, the LMS algorithm is widely used in many applications. Least – Mean - Square (LMS) adaptive filter is the main component of many communication systems; traditionally, such adaptive filters are implemented in Digital Signal Processors (DSPs). Sometimes, they are implemented in ASICs, where performance is the key requirement. However, many high-performance DSP systems, including LMS adaptive filters, may be implemented using Field Programmable Gate Arrays (FPGAs) due to some of their attractive advantages. Such advantages include flexibility and programmability, but most of all, availability of tens to hundreds of hardware multipliers available on a chip.

The LMS adaptive filter enjoys a number of advantages over other adaptive algorithms, such as strong behavior when implemented in finite-precision hardware,well understood convergence behavior and computational simplicity for most situations as compared to other adaptive algorithms.

Identifying an unknown system has been a central issue in various application areas such as control, channel equalization, echo cancellation in communication networks and teleconferencing etc. Identification is the procedure of specifying the unknown model in terms of the available experimental evidence, that is, a set of measurements of the input output desired response signals and an appropriately error that is optimized with respect to unknown model parameters. Adaptive identification refers to a particular procedure where we learn more about the model as each new pair of measurements is received and we update the knowledge to incorporate the newly received information.

The Least Mean Square (LMS) adaptive filter is a simple well behaved algorithm which is commonly used in applications where a system has to adapt to its environment. Architectures are examined in terms of the following criteria: speed,power consumption and FPGA resource usage.

Thesis Scope

This thesis will focus on FPGA implementation of the LMS Adaptive filter and verify it for using as a system identification of unknown system (FIR filter).The design of unknown FIR Filter was based on the use of FDATOOL in MATLAB which generates the VHDL code for the filter, also an optimized filter was made using VHDL code as another alternative. This thesis consists of five chapters, organized as follows:

Chapter One

This chapter presents a brief history of programmable logic devices from the simple beginning to their modern complex architectures. Current trends such as embedded DSP blocks are discussed, as well as the hardware description languages and tools that are used to program them.

Chapter Two

In this chapter we discuss an overview of the adaptive filtering problem and the various training algorithms

Chapter Three

In this chapter we discuss an overview of MATLAB implementation of various training algorithms also the implementation using SIMULINK, high level language like C.

Chapter Four

In this chapter we discuss the details of FPGA implementation of LMS filter for identifying unknown system using various techniques.

Chapter Five

In this chapter, we summarize the Results of this Thesis and propose the future work.