A LOW-COMPLEXITY FAST FOURIER TRANSFORM ARCHITECTURE

By

Ahmed Mamdouh Ahmed ElShafiy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

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Under the Supervision of

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Title of Thesis:

A Low-Complexity Fast Fourier Transform Architecture

Key Words:
Fast Fourier Transform (FFT); CORDIC; Multiple Constant Multiplication (MCM); Partial FFT; SQNR

Summary:
In digital signal processing field, it is often required to transform the signal between time and frequency domains using the Fast Fourier Transform (FFT) algorithm. Therefore FFT blocks is one of the basic building block in digital signal processors. The basic computational units of the high-throughput pipeline FFT architectures are the butterfly block and a rotator block. The butterfly block performs a weighted complex addition and subtraction, while the rotator block performs a rotation in the complex plane by a given rotation angles, i.e., the twiddle factors. Compared to the butterfly operation, the rotator operation is the costly one. In this work we propose a restructure to the conventional FFT rotational angles into a modified HardWare-Friendly FFT (HW-F FFT) angles. The main goal is to enhance either power, area or speed performance while maintaining the Signal to Quantization Noise Ratio (SQNR) requirements.

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Dedication

To my family and beloved fiancé Shereen who have always supported me during this work.

Table of Contents

List of Tables