

Ain Shams University Faculty of Engineering

Engineering Physics and Mathematics Department

Simulation and Modeling of Nanowire transistors

A THESIS

Submitted in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Engineering Physics

By **Dalia Selim Louis**

M.Sc. in Engineering Physics (Engineering Physics and Mathematics) Ain Shams University - 2007

Supervised by:

Prof. Dr. Omar Abd-El Halim OmarAin Shams University

Prof. Dr. Wael Fikry FaroukAin Shams University

Prof. Dr. Salah El-Din Hassan GamalAin Shams University

Cairo, 2012



Ain Shams University Faculty of Engineering

Engineering Physics and Mathematics Department Cairo, Egypt

EXAMINERS' COMMITTEE

Dalia Selim Louis Armanious

Name:

Date: .../2012

Thesis: Simulation and Modeling of Nanowire Transistors Degree: Doctor of Philosophy in Engineering Physics. Title, Name and Affiliation **Signature** Prof. Dr. Gusteau Duclos Electronics Engineering Technology (Chair) DeVry College of New York - USA Prof. Dr. Abd-El Halim Mahmoud Shousha Electronics and Communication Eng. Department Faculty of Engineering-Cairo University Prof. Dr. Omar Abd-El Halim Omar Engineering Physics and Mathematics Department Faculty of Engineering -Ain Shams University Prof. Dr. Salah El-Din Hassan Gamal Engineering Physics and Mathematics Department Faculty of Engineering -Ain Shams University

STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Engineering Physics.

The work included in the thesis was carried out by the author at the Engineering Physics and Mathematics Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

Name:	Dalia	Selim	Louis

Signature:

Date:

CURRICULUM VITAE

Name of Researcher Dalia Selim Louis Armanious

Date of Birth 12/12/1979

Place of Birth Kuwait

First University Degree B.Sc. in Electrical Engineering

Name of University Ain Shams University

Date of Degree 2001

Last Degree M.Sc. in Engineering Physics

Name of University Ain Shams University

Date of Degree 2007

ABSTRACT

Dalia Selim Louis, "Simulation and modeling of nanowire Transistors," Doctor of Philosophy dissertation, Ain Shams University, 2012.

Scaling challenges and performance are directing the research into new device structures in the nanoscale regime. Among these devices are the silicon nanowire transistors that had attracted broad attention from both the semiconductor industry and the academic researchers. This is attributable to its improved electrostatic control of the channel and consequent suppression for the short-channel effects. For the design and optimization of nanowire transistors numerical quantum-based device simulator is needed that helps to understand its physics and further enhance its behavior. It is worth mentioning that both computational efficiency and high accuracy, taking physical effects into consideration, are crucial in building a simulator.

The main objective of this work is to build a full numerical simulator for cylindrical nanowire transistors under MATLAB environment that can be used in the investigation of the device's properties and output characteristics with efficient simulation time. This simulator is based on the effective mass approximation and utilizes the cylindrical coordinate system in order to take the advantage of the symmetry in the φ – direction, thus, an isotropic effective mass has been introduced in the simulator. The objectives of this thesis are: 1) Investigating the quantization effects in nanowire transistors using a 1D self-consistent Poisson – Schrödinger solver in conjunction with a semi-classical current model; 2) Examining the upper performance limit of the transistor (ballistic case) through proposing a 2D numerical simulator that uses the mode space approach where the Non-Equilibrium Green's Function (NEGF) is used to solve the transport equation; 3) Studying the non-coherent transport via including a phenomenological model to the simulator. Accordingly, a complete simulator is achieved that has the great advantage of simulation time reduction while keeping high level of precision

Key Words: SNWTs, NEGF, Mode space, Isotropic effective mass.

ACKNOWLEDGMENT

No one who achieves success does so without the help of others.
The wise and confident acknowledge this help with gratitude.

Alfred North Whitehead

First and foremost, I would like to thank my greatest teacher of all: God. I know that I am here and that I am able to write all of this for a reason. I will do my best in never forgetting what a great fortune I have had in just being here, and that it comes with a lesson and a responsibility. I hope I am doing the work You have planned me to do.

I am specifically grateful to my Prof. Dr. Omar Abd-El Halim for his kind support and guidance that has been of great value in my academic life. Also, I wish to express my warm and sincere gratitude to Prof. Dr. Wael Fikry Farouk for always making himself available with useful tips despite his super busy schedules. Their ideas and concepts have had a remarkable influence on my entire career and I am sure will be of great help to me in my future professional life.

I am deeply indebted to my thesis supervisor, Prof. Dr. Salah El-Din Hassan Gamal for his help and advice through the course of my PhD study. His wide knowledge and his logical way of thinking have been of great value for me. His understanding, encouraging and personal guidance have provided a good foundation for the present thesis.

I warmly extend my thanks to Dr. Mahmoud Ibrahim, Dr. Mohamed El-Banna and Dr. Mona El-Sabbagh for the fruitful discussions we had together around my work area. And my old friend Dr. Michael Bebars, who have generously provided me with material and papers that were much needed for my research. During this work I have collaborated with many colleagues in our department for whom I have great regard, and I wish to extend my warmest thanks to all of them

Last but not least, I can't thank my husband Rafik, son Fady and my loving parents enough, without their support, encouragement and understanding it would have been impossible for me to finish this work.

CONTENTS

LIST OF FIGURES.	
LIST OF TABLES.	xxi
LIST OF SYMBOLS AND ABBREVIATIONS	
INTRODUCTION	1
1. Nanowire Transistors.	4
1.1 Introduction	4
1.2 General View of Nanowires.	5
1.2.1 What Is A Nanowire?	5
1.2.2 Nanowire fabrication	6
1.2.2.1 Top-Down Approach	6
1.2.2.2 Bottom-Up Approach	7
1.2.3 Nanowire Applications.	8
1.2.3.1 Nanowire Electronics.	9
1.2.3.2 Nanowire Batteries.	10
1.2.3.3 Nanowire Biosensors.	11
1.2.4 Why Nanowire Transistors?	12
1.3 Physics of Nanowire Transistors.	14
1.3.1Classical Effects.	14
1.3.1.1 Short Channel Effects and Natural Length	14
1.3.1.2 Current Drive.	15
1.3.2 Quantum Effects.	16
1.3.2.1 Volume Inversion.	17
1.3.2.2 Mobility Effects.	18
1.3.2.3 Threshold Voltage	19
1.4 Numerical Simulation of SNWTs	22
1.4.1 Self-consistent Simulation Method	22

1.4.2 Discretization Methods.	23
1.4.2.1 Finite Difference Method.	24
1.4.2.2Finite Element method	26
1.4.3 NEGF Formalism.	29
2. QUANTIZATION EFFECTS AND SEMI-CLASSICAL BALLISTIC TRANSPORT IN SNWTS.	35
2.1 Introduction.	35
2.2 Model	36
2.2.1 Poisson's Equation.	37
2.2.2 Schrödinger Equation.	41
2.2.3 Current Model	45
2.3 Results and Discussion.	47
2.3.1 Model Verification.	47
2.3.2 Quantization Effects [Gam10]	49
2.3.3 Ballistic Transport and $I - V$ Characteristics	54
3. SIMULATION OF COHERENT TRANSPORT IN SNWTS	59
3.1 Introduction.	59
3.2 Methodology	60
3.2.1 Simulated Device Structure	61
3.2.2 Poisson Solver	63
3.2.2.1 Finite Difference Method.	63
3.2.2.2 Finite Element Method	67
3.2.3 Transport Model.	69
3.3 Results and Discussion	74
3.3.1 Benchmarking the Proposed Simulator	74
3.3.2 Detailed Device Physics	77
3.3.3 Assessment of the Uncoupled Mode Space Approach	82

CONTENTS xiii

4. NON-COHERENT TRANSPORT IN SNWTS	87
4.1 Introduction	87
4.2 Dephasing Model	88
4.3 Results and Discussion	94
4.3.1 Internal Quantities.	94
4.3.2 Momentum Relaxing and Conserving Models	99
4.3.3 <i>I</i> – <i>V</i> Characteristics.	101
CONCLUSION AND FUTURE WORK	105
REFERENCES	107
APPENDIX A – ANALYTICAL SOLUTION OF SCHRÖDINGER EQUATION	115
APPENDIX B – EXPRESSIONS FOR DENSITY OF STATES, CARRIER DENSITIES AND CURRENT	120

LIST OF FIGURES

Figure 1.1	Transmission Electron Micrograph TEM of an InP/InAs nanowire [Bjk02]	6
Figure 1.2	Schematic for the Vapor-Liquid-Solid synthesis method	8
Figure 1.3	Schematic for diagram for a silicon nanowire transistor	9
Figure 1.4	(a) Schematic of morphological changes that occur in Si during electrochemical cycling (b) Schematic Si nanowire (NW) anode configuration [cha08]	10
Figure 1.5	Schematic of multiplexed protein detection by 3 silicon nanowire devices each attached by a distinct receptor. [Zhe05]	12
Figure 1.6	Progression of device structure from single-gated planar to fully GAA NW MOSFETs [Sin08].	13
Figure 1.7	$I_D - V_D$ Characteristics at $V_G = 0.7V$ for single, double, tri- and quadruple gate devices (SG, DG, TG and QG respectively) [Mar06].	15
Figure 1.8	$I_D - V_G$ Characteristics at $V_D = 0.7V$ for SG, DG, TG and QG transistors [Mar06].	16
Figure 1.9	Electron charge density for the SNWT with diameter 5nm and oxide thickness 0.9 nm at $V_G = 1.1V$ [Mar06]	17
Figure 1.10	Phonon-limited mobility as a function of applied bias for wire diameters 3, 5, 7, 10, and 15 nm. The dotted line shows mobility with the isotropic choice for the mass tensor. The solid line shows the mobility of the	18

	planar n-type MOS. [Kot04]	
Figure 1.11	Low-field mobility as a function of the radius of the nanowire calculated at effective electric field of 10kV/cm [Oss10]	19
Figure 1.12	Transfer characteristics for two GAA transistors with $T_{ox} = 1.5 \ nm \ [\text{Jim}04]$	20
Figure 1.13	The extracted threshold voltage comparison of the SRG MOSFETs between classical and quantum-mechanical numerical simulation for different silicon radii and fixed gate oxide thickness. [Bia09]	21
Figure 1.14	The extracted threshold voltage comparison of the SRG MOSFETs between classical and quantum-mechanical numerical simulation for different gate oxide thickness and fixed silicon radius. [Bia09]	21
Figure 1.15	Self-consistent scheme that is used in the SNWT simulation.	23
Figure 1.16	Estimates for the derivative of $f(x)$ at point P using central differences	24
Figure 1.17	Finite difference mesh for two independent variables x and y	25
Figure 1.18	Selectively refined finite difference mesh.	26
Figure 1.19	(a) Schematic representation of an isolated device (Closed System). (b) Schematic representation of a device interacting with a reservoir (Open System)	31
Figure 2.1	Schematic sketch for the GAA nanowire structure studied in this chapter	36
Figure 2.2	Set of points forming the grid in the radial direction in	38

LIST OF FIGURES xvi

	nanowire transistor.	
Figure 2.3	Schematic diagram of the energy band diagram of the silicon nanowire capacitor.	40
Figure 2.4	Constant energy surfaces for electrons in bulk Si.	42
Figure 2.5	A schematic diagram showing the semiclassical ballistic transport in a nanoscale FET.	46
Figure 2.6	Comparison between the obtained eigenfunctions both analytical and numerical for an infinite circular potential well of radius 3nm.	48
Figure 2.7	Comparison between the first four eigenenergies obtained both analytically and numerically for an infinite circular potential well with radii ranging from 2nm till 10nm.	48
Figure 2.8	Comparison of electron density distribution between classical model and quantum confinement model in silicon nanowires of radii 5 nm and 10 nm. The oxide thickness is 2 nm. The gate voltage is 0.8 V. Midgap gate is assumed.	49
Figure 2.9	Electron density distribution for a silicon nanowire of radius 2.5 nm.	50
Figure 2.10	Electron distribution profiles in Si-nanowires with oxide thicknesses 1 nm and 4 nm and radius 2 nm at $V_G=0.7V$.	50
Figure 2.11	Electron density per unit length versus the gate voltage for silicon nanowires of radii 5 nm and 10 nm. The oxide thickness is 2 nm and Midgap gate is assumed	51
Figure 2.12	Surface potential \emptyset_s and body center potential \emptyset_0 versus the gate voltage. The oxide thickness is 2 nm and	52

Figure 3.6

	Midgap gate is assumed	
Figure 2.13	$C-V$ characteristics computed classically C_{cl} and quantum mechanically C_Q . The oxide thickness is 2 nm and Midgap gate is assumed.	53
Figure 2.14	Dependence of the threshold voltage on the nanowire diameter.	53
Figure 2.15	(a) Dependence of the electron injection velocity on the nanowire diameter. (b) the first band occupation factor versus the nanowire diameter. All quantities are evaluated at gate overdive $0.6\mathrm{V}$	55
Figure 2.16	$I_D - V_D$ at $V_G - V_t = 0.8V$ for two nanowires of radii 1 nm and 5 nm respectively.	56
Figure 2.17	(a) $I_D - V_D$ characteristics of a Si-nanowire with radius 3 nm and oxide thickness 1 nm. (b) The transfer characteristics of the same transistor.	57
Figure 3.1	A flowchart for the 2D simulator for ballistic cylindrical SNWTs.	60
Figure 3.2	Schematic structure of SNWT simulated in this work. (a) Lateral view, (b) Cross section, (c) Grid spacing in z-direction, (d) Grid spacing in radial direction.	62
Figure 3.3	2D mesh in the r-z plane of the SNWT	64
Figure 3.4	Flatband voltage versus the nanowire length with constant nanowire diameter 3nm.	75
Figure 3.5	Flatband voltage versus the nanowire diameter with constant channel length 10 nm.	75

 $I_D - V_G$ Characteristics of nanowire transistor with 76

diameter 3.2 nm and channel length 10 nm.

LIST OF FIGURES xviii

Figure 3.7	$I_D - V_G$ characteristics of nanowire transistor with diameter 4.5 nm and channel length 10 nm .	77
Figure 3.8	1D electron density for the first four subbands in a nanowire of diameter 4.5 <i>nm</i> . The dotted horizontal line represents the predefined criterion for the minimum charge density to be included in the calculations.	78
Figure 3.9	LDOS and electron subbands (solid white lines) for the simulated nanowire at $V_G = V_D = 0.4V$.	79
Figure 3.10	The 2D electron wavefunctions in the cross section of the simulated transistor for the first 6 modes at $V_G = V_D = 0.4V$.	79
Figure 3.11	The 1D electron density profile along the channel of the simulated device.	80
Figure 3.12	The transmission coefficient and the energy subbands along the channel of the simulated device.	81
Figure 3.13	The conduction band edge along the channel of the simulated device at $V_G = V_D = 0.4V$.	81
Figure 3.14	The 3D electron density in the $r-z$ cross section of the simulated device at $V_G = V_D = 0.4V$	82
Figure 3.15	First eigenfuction $\rho^1(r)$ versus the radial distance at different points along the channel direction for a nanowire transistor of diameter 4.5 nm $L=10 nm$ and at a bias point $V_G=V_D=0.5V$	83
Figure 3.16	First eigenfuction $\rho^1(r)$ versus the radial distance at different points along the channel direction for a nanowire transistor of diameter $8 nm$ and $L = 12 nm$ at a bias point $V_G = V_D = 0.5V$.	84
Figure 4.1	A flowchart for the 2D simulator for dissipative	93

	cylindrical SNWTs.	
Figure 4.2	(a) Local density of states LDOS in the ballistic case at $V_D = V_G = 0.4V$. (b) LDOS in the momentum relaxing case	95
Figure 4.3	(a) The charge density spectrum from the ballistic model. The charge density spectrum from the dissipative model (momentum relaxing).	96
Figure 4.4	Simulated energy spectrum of the current at the source and drain ends for both ballistic and dissipative cases at high bias $V_G = V_D = 0.4V$	98
Figure 4.5	Simulated energy spectrum of the current at the source and drain ends for both ballistic and dissipative cases at low bias $V_G = V_D = 0.1V$. the vertical line represents the source to channel barrier	98
Figure 4.6	Transmission coefficient in case of ballistic, momentum relaxing and momentum conserving transport models with two scatterers placed in the channel (with energy $0.5 \ eV \ e$ each). $d_m = d_p = 0.012 \ eV^2$.	100
Figure 4.7	Simulated energy spectrum of the source current in case of ballistic, momentum relaxing and momentum conserving transport models at $V_G = V_D = 0.4V$.	100
Figure 4.8	$I_D - V_D$ characteristics for SNWT with diameter 3 nm and channel length 10 nm for both the ballistic and dissipative transports. ($d_m = 0.01 eV^2$)	101
Figure 4.9	$I_D - V_G$ characteristics for SNWT with diameter 3 nm and channel length 10 nm for both the ballistic and dissipative transports. ($d_m = 0.01 eV^2$)	102
Figure 4.10	Ballisticity versus the channel length for a SNWT of diameter 3 nm	103