Ain Shams University
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Graph Based Techniques Applied in Electrical Circuit Simulation

A Thesis

Submitted in partial fulfillment for the requirements of Doctorate of Philosophy of Science degree in Electrical Engineering

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Abstract

In this dissertation, the acceleration of electrical circuit simulation problem is addressed. As SPICE simulator core engine is the base of most current electrical circuit simulator, this engine is studied for detecting performance bottlenecks. Due its time complexity, solving sparse matrix step in SPICE engine is targeted in this dissertation to enhance the performance of the simulator.

A novel technique based on graph theory is introduced to solve sparse linear systems. The proposed technique enhances the ability to build sparse parallel solvers for circuit simulation matrices. Thus the proposed technique accelerated the performance of circuit simulation algorithms. The new technique represents sparse linear system as a signal flow graph (SFG). Then it divides the graph into separate strongly connected components (SCCs). SCCs relations are detected and represented in reduced graphs which are used to enhance the parallelism of the solver. To benefit from the parallel nature of the reduced graph representation, Graphics Processing Unit (GPU) is used to accelerate sparse Lower Upper (LU) factorization.

The main contribution in this dissertation is the parallelization of KLU ("Clark Kent" LU) algorithm through introducing the concept of the reduced graph. A theory that states that Reduced Graph are Non-Cyclic and hence can be processed in parallel is introduced and proved. The GPU is used to implement proposed parallel KLU. To validate the performance of the proposed technique, it is tested against real circuit matrices from the University of Florida sparse matrix collection. The proposed technique outperformed sequential KLU in most of the test cases.

Statement

This dissertation is submitted to Ain Shams University for the degree of Doctor of Philosophy in Electrical Engineering (Computers and Systems Engineering).

The work included in this thesis was carried out by the author at the Computers and Systems Engineering Department, Faculty of Engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or qualification at other university or institution.

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List of Abbreviations

AMD	Approximate Minimum Degree
BLAS	Basic Linear Algebra Subprograms
BTF	Block Triangular Form
COLAMD	Column Approximate Minimum Degree
CUDA	Compute Unified Device Architecture
FPGA	Field Programmable Gate Array
GPU	Graphical Processing Unit
IC	Integrated Circuit
KCL	Kirchhoff's Current Law
KLU	Clark Kent Lower Upper
LU	Lower Upper
MNA	Modified Nodal Analysis
SCC	Strongly Connected Component
SFG	Signal Flow Graph
SIMD	Single Input Multiple Data
SIMT	Single Input Multiple Threads
SM	Streaming Multiprocessors
SoC	System on Chip
SP	Streaming Processor

SPICE	Simulation Program with Integrated Circuit Emphasis