Ain Shams University
Faculty of Engineering
Electronics and Communications Department

High Performance Analog to Digital Converters

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

Submitted by:

Michael Sherif Sobhy Nagib

B.Sc. of Electrical Engineering
(Electronics and Communications Department)
Ain Shams University, 2006.

Supervised by:
Prof. Dr. Hisham Haddara
Dr. Ayman El-Sayed

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Curriculum Vitae

Name: Michael Sherif Sobhy Nagib
Date of Birth: 12/9/1984
Place of Birth: Cairo, Egypt
First University Degree: B.Sc. in Electrical Engineering
Name of University: Ain Shams University
Date of Degree: June 2006

Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).
The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.
No part of this thesis was submitted for a degree or a qualification at any other university or institution.

Name: Michael Sherif Sobhy Nagib
Date: 12/1/2014

Abstract

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The hand-held/portable consumer electronics market has witnessed a huge growth through the last decade, fueled by the continuous innovation and improvement in the performance and applications of a variety of devices such as smart-phones, tablets, portable gaming-consoles and digital cameras.

One of the main common components in all those devices is the Analog-to-Digital converter found on almost every Integrated-Circuit within the device. The ADC is a crucial element that by large considered the bottleneck of the overall performance and power consumption of systems and devices, therefore creating a continuous demand for new ways to enhance the ADC performance and power consumption in order to open the door for new applications and features.

The Successive-Approximation (SAR) ADC architecture has started to gain vast interest in low-power applications, especially in new deep-submicron technology nodes. Although commonly known to be a challenging task to simultaneously push the resolution and speed of the SAR architecture mainly due to the sequential nature of the successive-approximation algorithm , yet a number of recent publications are overcoming this limitation by exploring several techniques to push the performance of the SAR ADCs beyond common-limits to fit within the consumer electronics applications such as broadband wireless communication (LTE,WiMAX,802.11a/b/g) and digital TV (DVB,DMB,ISDB) applications among many other applications that require medium resolution (10-12 bits) and medium speed (tens of MSPS) at the minimum possible power consumption for a longer battery life.

The work presented in this thesis is an attempt to study the different aspects of designing a successive-approximation (SAR) analog-to-digital converter

for hand-held consumer electronics applications with special emphasis on enhancing the power efficiency. The main target specifications is a 12-bit resolution at a sampling speed of 20-40MSPS. The main work flow included three phases, presented in chapters three, four and five of this thesis.

Chapter three starts by the system-level design and analysis where different architectural design aspects are explored and studied with the main aim of reducing the SAR ADC power consumption. The actual top-down implementation of the converter is covered in chapter four and finally a redundancy-based technique to further enhance the power/speed efficiency of the ADC is studied and implemented through the introduction of a novel feedback-DAC architecture in order to reduce the digital processing overhead associated with the redundancy technique as presented in chapter five.

In order to understand , assess and optimize the different trade-offs in the design of SAR converters , mixed-signal VHDL-AMS behavioral models were developed for all the main building blocks at different levels of abstraction. The behavioral models were used heavily in studying and justifying top-level architectural trade-offs as well as verifying the performance of the different building blocks within the complete system.

The ADC was implemented in $0.13\mu m/1.2$V technology with a reference buffer driving strength that can be easily programmed through variable current to be used to trade-off between the converter speed and power consumption.

Key words: ADC, successive-approximation, low-power, broadband wireless communication, LTE,WiMAX, 802.11a/b/g, digital TV, DVB, DMB, ISDB, redundancy, novel feedback-DAC architecture, variable strength reference buffer.

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Above all, I thank God for giving me the enthusiasm, guidance, determination and strength to start and complete this work.

Michael Nagib
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Thesis Summary

The work presented in this thesis is an attempt to study the different aspects of successive-approximation (SAR) analog-to-digital converters design and optimization with the main focus on enhancing the speed/power efficiency.

The thesis is divided into six chapters as listed below:

Chapter 1 : Introductory chapter highlighting the motivation behind this work and a brief description of the thesis outline and organization.

Chapter 2 : An introduction to the basics of Analog-to-Digital conversion in terms of terminology , specifications , figure-of-merits and challenges in the design of Analog-to-Digital converters as well as an overview of the different ADC architectures.

Chapter 3 : Focus on top-level system design and analysis of the SAR ADC by first providing an overview of the main building blocks followed by analysis of architectural level definition, design and trade-offs. The chapter concludes by budgeting noise and time on the different building blocks.

Chapter 4 : Presents the actual implementation of the converter starting from the top-level hierarchy definition and Analog/Digital segmentation down to the transistor-level implementation of each of the converter building blocks.

Chapter 5 : Focus on techniques that can be applied to the SAR converter in order to enhance its speed/power efficiency by first assessing the gain from those techniques and then implementing those techniques and comparing the results to that achieved with the conventional SAR architecture.

Chapter 6 : Conclusion and summary of the findings of this work as well as suggestions and proposal for future work.

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