Ain Shams University
Faculty of Engineering
Electronics and Electrical Communication

# Layout Dependent Effects on Nanometer IC Designs

## A Thesis

Submitted in partial fulfillment for the requirements of
Doctor of Philosophy Degree in Electrical Engineering
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بسم الله الرحمن الرحيم

# Statement

This thesis is submitted in partial fulfillment for the requirements of Doctor of Philosophy Degree of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

**Haitham Mohamad Abd ElHamid Eissa**

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# Abstract

As VLSI technology pushes into using advanced nodes down to 7nm and below, designers and foundries have exposed to a significant set of yield problems. To combat yield failures, the semiconductor industry has deployed new tools and methodologies commonly referred to as design for manufacturing (DFM). Most of the early DFM efforts concentrated on catastrophic failures, or physical DFM problems. However a new area of yield failures are now related to reliability and performance of the manufactured circuits, and having increased emphasis on what is now called "Parametric Yield" issues, and sometimes referred to as electrical-DFM (eDFM).

This thesis presents the parametric yield problems due to physical layout parameters effects on the final circuit performance, with more focus on their effects on Analog and Mixed signal (AMS) integrated circuits (ICs). These layout effects are generally known as Layout Dependent Effects or (LDEs). These parameters have to be considered in the design cycle and to be back annotated into the schematics or layout for accurate simulations. Thesis presents a complete eDFM solution that detects, analyzes, and fixes electrical hotspots (e-hotspots) within an analog circuit design, those caused by different process variations. Novel algorithms are proposed to implement the engines used to develop this solution. The flow is granted a US patented as of 2014.

The solution is examined on different designs, and at different technology nodes, including a 130-nm parametrically-failing level shifter circuit used in USB IP, which is verified with silicon wafer measurements that confirm the existence of parametric yield issues in the design. Additional experiments are applied on a 65-nm industrial operational amplifier and voltage control oscillator (VCO), as well as 45nm digital standard cell design. E-hotspot devices with high variations in dc current are identified. After fixing the e-hotspots, the variations in these designs are dramatically reduced to within designer's acceptance criteria, while saving the original circuit specifications.

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