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Design and Implementation Decimator for Bandpass Sigma Delta Modulators

A Thesis

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

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Abstract

This research work reports on the results obtained for the design and synthesis of a decimator for bandpass sigma-delta converters. The modeling is carried out structurally to get maximum impact on the system's design.

At first, three structures of bandpass filters for the decimator, namely; cascaded BPF-LPF, complex LPF, and narrow-band BPF were investigated. The investigation concentrates on the number of taps and the degradation in the in-band noise after decimation. The less degradation for the in-band noise, the more efficient anti-aliasing structure we have. That is the less the number of filter taps, the less power consumption of the structure is achieved. Extensive comparison between cascaded BPF-LPF and complex LPF structures were conducted. The comparison factors considered were computational effort for multiplications and additions per second, for multistage architectures. A set of MATLAB functions and SIMULINK models were developed. These functions perform ideal in-band noise estimation, in-band noise calculation before and after decimation, polyphase and halfband filter design, multistage filter design, exporting filter coefficients and test benches in appropriate format for VHDL implementation and testing. Complex LPF structures showed efficient structure for bandpass decimation. That is these structures have less filter taps, minimum in-band noise degradation after decimation, and minimum computational effort.

The VHDL model for the complex LPF structure for bandpass decimation was designed for a sampling frequency of 1.5MHz, decimation factor 64, 3 stages of decimation, 1-bit input bit width, and 16-bit output bit width.

The designed model was successfully synthesized using a UMC 0.18um technology and Xilinx Virtex-II FPGA. Which met the design requirements and performs stable timing simulation. Finally, the design was implemented using Xilinx Virtex-II FPGA successfully.

Keywords: Decimation, Polyphase Decimator, Bandpass, VHDL

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List of Abbreviations

Abbreviation	Meaning
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
ICs	Integrated Circuits
VLSI	Very Large Scale ICs
VHDL	Very Large Scale ICs Hardware Description Language
DSP	Digital Signal Processing
BPF	Bandpass Filter
LPF	Lowpass Filter
$\Sigma\Delta$	Sigma-Delta Modulator
LP $\Sigma\Delta$	Lowpass Sigma-Delta Modulator
BP $\Sigma\Delta$	Bandpass Sigma-Delta Modulator
PPD	Polyphase Decimator
CT	Continuous Time
DT	Discrete Time
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
HB	Halfband
APS	Additions Per Second
MPS	Multiplications Per Second
IF	Intermediate Frequency
BB	Baseband Frequency
NB	Narrow-Band