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Electronics and Communications Engineering Department

Design of a Clock Multiplier System

A Thesis

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Submitted by

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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Clock Multipliers are widely used in all digital systems, there is different architectures used to generate this clock, the need to minimize jitter in this clock is a must, there is techniques to minimize jitter .In this dissertation one of this techniques were used.

This dissertation starts with a survey on different architecture used as a clock multiplier then it concentrates on multiplying DLL architecture, a survey on previously implemented MDLL was made.

Next in this dissertation is the linear model of the multiplying DLL and it was used to extract loop parameters and to predict the total phase noise and in consequence the jitter .Linear model was assuming the loop to work as a PLL or DLL.

Next, the dissertation presents the implementation of a complete time domain model of the MDLL and from this model, different block requirements were extracted .The linear model was implemented using VerilogA language .

Next , the circuit implementation was made for all blocks in the MDLL , each block was designed and simulated and verified in the system , and at the end a verification of the whole system was made in the MDLL mode and PLL mode .All circuit implementation was done using 0.13um technology node .Simulation was done using Spectre .

Key words: Multiplying DLL , PLL , Clock Multiplier , Realignment VCO, Low Jitter Clock .

SUMMARY

This dissertation demonstrates the different issues of implementing a clock multiplier for digital applications. The dissertation is divided into four chapters and appendix organized as follows:

Chapter One: This chapter is introduction to clock multipliers. Survey on the multiplying DLL architecture was introduced.

Chapter Two: In this chapter, a linear model was implemented using Matlab for the multiplying DLL to extract loop parameters and to predict the overall phase noise and jitter.

Chapter Three: In this chapter, a time domain model was implemented using verilogA model, and the specs for each block were extracted from this model.

Chapter Four: In this chapter, circuit implementation of all blocks in the multiplying DLL. All the circuits were designed; analyzed and simulated .At the end of this chapter, verification of the whole system on the circuit level was shown.

Appendix: In this Appendix, the verilogA code was attached

Finally, the thesis ends by extracting conclusions and stating future work that may be done based on this work.

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