A DETERMINISTIC AND ACCURATE DYNAMIC POWER ESTIMATION METHOD FOR CMOS LOGIC CIRCUITS

By

Omnia Sayed Ahmed Fadl

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
DOCTOR OF PHILOSOPHY
in
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A deterministic and accurate dynamic power estimation method for CMOS logic circuits

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CMOS logic circuits; Logic pictures; Power estimation; Delay models; Switching activity.

Summary:

CMOS Integrated Circuits currently have very small geometrical features which lead to very high transistor density per chip. Consequently, a very important parameter in the design cycle is power consumption. With the proliferation of battery-operated devices, designing a circuit with low power consumption has become a must.
In general, it is essential for a designer to use a CAD tool that can quickly and accurately predict the circuit's power consumption. Existing CAD tools suffer from one main drawback, namely accuracy. This thesis aims at producing a CAD tool whose main advantage is accuracy. The technique used is the Logic Pictures (LPs). A Logic Picture is defined as the set of logic values at all gate outputs in the circuit for a given input vector. A deterministic and accurate method to calculate the nodes' toggle rate of CMOS logic circuit is presented. The nodes' toggle rate can be related directly to the dynamic power consumption of the circuit due to the charging and discharging of the load capacitances. The contributions of the thesis are the study of Logic Pictures in the context of combinational and sequential circuits. The unit-delay model is used first where the tool is applied to several standard/non-standard benchmark combinational circuits. The power consumption produced by the tool is compared to exhaustive simulations as well as Monte Carlo simulations. It is proven that the tool produces accurate results. The tool is then enhanced by using the real-delay model that closely matches the real-world circuits. Again, it was verified that it indeed produces accurate results.

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Nomenclature

CMOS	Complementary Metal-Oxide-Semiconductor
CAD	Computer-Aided Design
LP	Logic Picture
LG	Logic Group
VLSI	Very-Large-Scale integration
ABB	Adoptive Body Biasing
IRSIM	Incremental MOS Switch Level Simulator
RC	Resistor-Capacitor
I	Current
i_s	Reverse saturation current
V_{DD}	Diode voltage
Q	Electron's charge
K	Boltzmann's constant
T	Temperature
P	Power
T_{clk}	Clock period
A	Toggle rate
X	Undetermined logic
S	Switching activity
N	Estimate of the circuit gates count
K	Number of logic pictures
r, R	The logic picture repetition
Tr	Transition indicator
Δ	Propagation delay
S	Number of states
T_i	Time instant i

Abstract

CMOS Integrated Circuits currently have very small geometrical features, which leads to very high transistor density per chip. Consequently, a very important parameter in the design cycle is the circuit power consumption. With the proliferation of battery-operated devices, designing a circuit with low power consumption has become a must. Furthermore, it is well-known that high power consumption has a detrimental effect on system reliability due to overheating.

In general, it is essential for a designer to use a CAD tool that can quickly and accurately predict the circuit's power consumption. Existing CAD tools suffer from one main drawback, namely accuracy. Some of these tools are simulation-based; a subset of the input vectors is used to predict power consumption. This prediction just produces an estimate which is biased to the input vectors chosen. Other tools are non-simulation-based methods and are based on probabilistic approaches which suffer from the uncertainty of the probabilistic approaches.

Besides the computational complexity and the memory space required, these afore-mentioned tools all produce power consumption estimates, i.e., they are not very accurate. This thesis aims at producing a CAD tool whose main advantage is accuracy. The technique used is the Logic Pictures (LPs). A Logic Picture is defined as the set of logic values at all gate outputs in the circuit for a given input vector. A deterministic and accurate method to calculate the nodes' toggle rate of CMOS logic circuit is presented. The nodes' toggle rate can be related directly to the dynamic power consumption of the circuit due to the charging and discharging of the load capacitances.

The first contribution of the thesis is the study of Logic Pictures in the context of combinational circuits. The unit-delay model is used first where the tool is applied to several standard/non-standard benchmark combinational circuits. The power consumption produced by the tool is compared to exhaustive simulations as well as Monte Carlo simulations. It is proven that the tool produces accurate results. The tool is then enhanced by using the real-delay model that closely matches the real-world circuits. Again, it was verified that it indeed produces accurate results. It was also shown that the tool was much faster than exhaustive simulations. The memory space saving is up to a ratio of 30.1% (saving memory is defined as the ratio between the vectors needed for exhaustive simulations and the vectors used in the proposed method) and the time saving is up to 96% for highly regular circuits compared to the time used in exhaustive simulations. Finally, the tool is used to provide recommendations to the designer in terms of the best gates layout options that produce minimum power consumption.

The second main contribution of the thesis deals with sequential circuits. It is a known fact that switching in sequential circuits is much more complex than in combinational circuits due to the existence of State elements (Flip-Flops) that can be

considered as secondary inputs where State feedbacks complicate the analysis drastically. Again, both the unit and real-delay models are used. In order to prove the method's efficiency, it was applied to different standard/non-standard circuits and the results are compared to both exhaustive and Monte Carlo simulations. It is shown that the results were found to be identical to the accurate exhaustive simulations but with much lower processing time and much lower memory space requirements especially for regular circuits. Time saving of up to 97.2% for highly regular circuits is achieved compared to exhaustive simulation time. Further time saving is achieved by using a C++ version of the tool, instead of the MATLAB one. Together with accepting some data truncations errors, this reduced the processing time by at least two orders of magnitude.

Chapter 1 : Introduction

With the new trends in portable electronic devices, an extra need arises for cooling devices which matches the higher density of transistors in smaller areas and the problems of extending battery life. Power dissipation has therefore become an important parameter in VLSI circuits design along with area and speed [1, 2]. Technologies that depend on CMOS were originally developed because CMOS power consumption is less than other equivalent devices but relaying on this idea alone is not enough. Power calculations are necessary to determine the maximum operating frequency, sizing of the power supplies and selection of the suitable device [3]. High power consumption can cause major device damages and may lead to runtime errors, which affects the circuit reliability and lifetime. Hence, along with low power design techniques at different level of circuits design, accurate power estimation tools at any design level are highly needed.

For CMOS devices, there are two power consumption sources which are static and dynamic power consumption. Static power consumption happens when the transistor is either ON or OFF state. It is the result of the leakage currents in the device and these leakage components depend mainly on the device geometry, temperature, and doping levels. Static power can be minimized by careful design techniques. Dynamic power consumption happens when the transistor is changing its state of operation from ON to OFF or vice versa. It consists of three components: leakage power, short circuit power and switching power. Leakage and short circuit power are design dependent but the switching power consumption depends on the circuit operation and design structure [4-6].

Switching power is due to charging and discharging of the CMOS circuit node load capacitance during the node transition. It is the dominant source of dynamic power consumption. The nodes toggle rate is a sufficient indication of the circuit switching power consumption [7-12] and this thesis focuses on a deterministic and accurate method to estimate its value.

Many average power estimation methods have been developed over the years; they can mainly be divided into two main categories. First, there are simulation-based methods [13-23] which rely on simulating the circuit with an appropriate set of inputs to obtain the power consumption. The main problems in simulative-based methods are the large memory requirements, time consumption and finding the suitable input vector set needed to exercise the circuit. Second, there are non-simulation based methods [24-35] which depend on probabilistic measures for the inputs and the switching activities to find the power consumption. While being efficient for large circuits with acceptable margins of errors, the power produced is not accurate but only an estimate.

There is a compromise between speed and accuracy when choosing a power estimation method. Existing power estimation methods are either accurate but

impractical for large circuit or fast but with the cost of lower accuracy. Since reliability is a big issue in the design phase there are different proposed methods to estimate maximum power consumption [36-44].

In this thesis, the accuracy problem is solved by simulating the circuit for all possible scenarios in different time instants. To avoid the errors in calculations, unit-delay and real-delay models algorithms are provided for combinational and sequential logic CMOS circuits. To speed the calculation process, the idea of logic pictures of the circuit nodes is used. A Logic Picture (LP) consists of the steady state values of all gates outputs (nodes) for a certain input combination [45-50]. The maximum possible number of LPs for an n-input circuit is 2^n LPs, but experimentally their actual number is much smaller than 2^n.

Finding the dynamic power using exhaustive testing requires 2^{2n} simulation cycles to cover all the circuit transitions, but obtaining LPs for n-input circuits require only 2^n simulation cycles. This means that acquiring the dynamic power using LPs has lower complexity than that of exhaustive testing. Moreover it needs less memory space. Since the LP count is relatively small, LPs were used in calculating the switching activity; the nodes' toggle rate and hence average switching power were obtained. Also as the regularity of the circuit increases, the ratio of the number of logic pictures compared to the size of the truth table entries (2^n) decreases.

For CMOS circuits, LPs are acquired directly from the truth/state table of the circuit. Logic groups that contain the inputs that lead to the LPs are then formed. Inputs from different logic groups other than the logic group that contains the initial LP are applied to the circuit. Unit-delay models and real-delay model were assumed for the circuits' gates and the simulations cover the intermediate LPs that may arise because of the circuit gate delays. The toggle rate of the circuit nodes is calculated from the LPs probabilities through different time instants of circuit operation.

To validate the results of proposed algorithm, it was applied to different selected standard and non standard CMOS logic circuits. The outputs of the proposed method were compared to exhaustive and Monte Carlo simulations outputs in terms of time usage and saving memory. The simulations tools are MATLAB 2013a and Microsoft Visual Studio 2010. The results were found to be identical to the exhaustive simulations output but with much lower complexity and memory space requirements. The memory space saving is up to 30.1% and the time saving is up to 96% for highly regular circuits.

1.1. Organization of the thesis

The remainder of this thesis is organized as follows. Chapter 2 is a detailed survey of previous studies. It contains a review of the sources of power consumption in CMOS digital circuits with a comprehensive explanation. It also details other work done in the field of power estimation and the related work to this thesis. Chapter 3 provides an explanation of the proposed power estimation method for combinational circuits for unit-delay model gates and real-delay model. Chapter 4 introduces the proposed power

estimation method for sequential circuits also for unit-delay model gates and real-delay model. Chapter 5 shows the experimental results compared to exhaustive and Monte Carlo simulations. Finally the Conclusion Section summarizes the thesis work.