AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Analog-to-Digital Converter for Wireless Sensor Network Applications

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Amr Ibrahim Farag Eissa

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2012

Supervised By

Prof. Hani Fikry Ragai

Dr. Mohamed Ahmed Mohamed El - Nozahi

Cairo – (2016)

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications

Analog-to-Digital Converter for Wireless Sensor Network Applications

by

Amr Ibrahim Farag Eissa

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2012

Examiners' Committee

Name and Affiliation	**Signature**
Prof. Dr. El-Sayed Mostafa Saad Electronics Engineering and Electrical Communications Faculty of Engineering, Helwan University	……………….
Prof. Dr. Mohamed Amin Dessouky Electronics Engineering and Electrical Communications Faculty of Engineering, Ain Shams University	……………….
Prof. Hani Fikry Ragai Electronics Engineering and Electrical Communications Faculty of Engineering, Ain Shams University	……………….

Date: 19 August 2016

Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain Shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Amr Ibrahim Farag Eissa

Signature

…………...……….

Date: 17 August 2016

Researcher Data

Name	: Amr Ibrahim Farag Eissa
Date of birth	: 09/26/1990
Place of birth	: Cairo, Egypt
Last academic degree	: Bachelor of Science
Field of specialization	: Electronics Engineering
University issued the degree	: Ain Shams University
Date of issued degree	: July 2012
Current job	: Teaching & Research Assistant at the Faculty of Engineering, Ain Shams University.

Thesis Summary

Faculty of Engineering – Ain Shams University

Electronics and Communication Engineering Department

Thesis title: "Analog-to-Digital Converter for Wireless Sensor Network Applications"

Submitted by: Amr Ibrahim Farag Eissa

Degree: Master of Science in Electrical Engineering

The realization of wireless sensor networks (WSN) put stringent requirements on its different building blocks. Among different blocks, the analog-to-digital converter (ADC) design proves to affect the overall system performance, especially in systems employing complex digital signal processing (DSP) algorithms. Static offset, clock jitter, signal-to-noise ratio (SNR), and system linearity are examples of different system specifications that directly impact the ADC design. In this thesis, the main focus is the design of an ADC for WSN application, implemented in CMOS technology.

The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references and the appendices.

Chapter 1

Chapter 1 introduces the main motivations beyond digital domain processing and the driving factors. A brief outline of various ADC applications is presented with major focus on wireless sensor networks harassed for bio-medical applications such as ECG signals monitoring. The chapter ends by clearly identifying the main challenges imposed on ADC design in such systems regarding power and area requirements, clearly identifying the proper context of this work.

Chapter 2

Chapter 2 aims to provide a quick refresher in regard of the basic ADC systems and the encountered signal processing steps. It goes further with brief discussions clarifying the main performance metrics and terminologies used in the world of ADCs. The rest of the chapter is devoted to a quick literature review on the basic ADC architectures, their main operation principles, non-idealities, and recent innovations and state-of-the art architectures.

Chapter 3

Chapter 3 starts by briefly recapping the main challenges obviating SAR and Sigma-Delta ADCs from achieving high power efficiencies at high resolutions. The theory of feed forward noise shaping (FFNS) is proposed, generally as a new ADC architecture in which the noise shaping is achieved without placing the main quantizer in a feedback loop, and specifically, as a hybrid solution that merges the high power efficiency of SAR ADCs with the high resolution capabilities of noise shaping, along with benefiting from the basic idea of digital error correction incorporated in pipelined ADCs.

Behavioral system models have been developed along with the appropriate quantitative analyses to support the proposed idea. System block diagrams for first and second order FFNS based ADCs have been extracted and generalized to L^{th}-order FFNS architectures. Finally, the theory of FFNS has been extended to build up partially oversampled FFNS-based ADCs.

Chapter 4

Chapter 4 deals with the design considerations of the proposed FFNS-based system. SAR ADCs have been chosen as core quantizers owing to their high power efficiencies. The chapter starts by revisiting the bio-medical application under question, and conducting a power budget for a given set of specifications. A quantitative comparison between the Conventional Binary Weighted (CBW) and Binary Weighted DAC with Attenuating capacitor (BWA) switching schemes have been conducted showing that the former is more superior to the latter, in terms of area and power consumption, when linearity requirements are taken into account.

The chapter proceeds, afterwards, by conducting a quantitative power driven model for the proposed FFNS system.

Chapter 5

Chapter 5 presents the design details of 1^{st} order FFNS and PO-FFNS based ADCs. For each system, a proposed circuit implementation is proposed along with carefully analyzing non-idealities effects. Detailed design of all sub – blocks is presented along with overall system simulations.

Chapter 6

Chapter 6 presents a summary for the dissertation, along with possible directions for future work.

Key words: SAR ADCs, Sigma – Delta ADCs, Low Power, Biomedical CMOS ICs, Noise – shaping.

Acknowledgments

All praise is due to ALLAH, the most gracious, the most merciful, for His generosity; without Whom I wouldn't have reached this point in my life.

My special thanks go first to my family who generously supported me throughout all my life. Special thanks to my parents; there are absolutely no words or actions through which I can pay them back the tiniest of their favors, sacrifices, kindness, and support. My cordial thanks then go to my wife, who carried on her shoulders the heavy burden of supporting me through every step; thank you for all the sacrifices you have made to keep all of us happy.

My sincerest thanks go to Prof. Hani Fikry for supervising my MSc thesis and for taking a genuine care of my work and providing suggestions, directions, and technical and moral support whenever I needed.

I cannot extend enough thanks to my exceptional mentor, Dr. Mohamed El-Nozahi, whose guidance and surveillance are the reasons I'm able to write the lines of this work. My deep appreciations go to his kindness, motivation, patience, and for introducing me to IC design. I really owe him a lot.

I would like, also, to thank Prof. Amr Safwat who had a major role in my early formation and interaction with the field of electrical engineering, aside from his precious advices, and fruitful discussions.

I would also like to thank all my colleagues at the Integrated Circuits Lab (ICL) at Ain Shams University for their continuous support.

Finally, I would like to thank Prof. El-Sayed Mostafa Saad and Prof. Mohamed Dessouky for being my thesis examination committee.

Amr Ibrahim Farag Eissa

Electronics Engineering and Electrical Communications

Faculty of Engineering, Ain Shams University

Cairo, Egypt

August 2016

Contents