AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Computer and Systems Engineering

Assertion-based Verification for Inter-Device Communication in System-on-Chip

A Thesis submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Computer and Systems Engineering)

by

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Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Date: 10 August 2017

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Abstract

Communication between devices on-chip takes place through bus interfaces and bus interconnect logic. Usually communication involves master and slave devices cross-talking by protocols defining when to send and receive the data and how the data should look like. Communication protocols could be standard or customized according to the chip design firm. Connecting or integrating such masters, slaves and interconnect in the system-on-chip is often an automatic process that involves scripting work, which in turn may involve mistakes. Devices communication may involve controlling or configuring devices and probing their statuses. In that case devices are looked at as memory mapped, and communication takes place so that devices configuration and status registers are read and written through transactions communicated on the device bus interface. The hardware description of the memory mapped devices is often automatically generated from a standard description of the registers, and consequently a percentage of failure rate comes from the nature of automation that may involve mistakes.

This research work is concerned with two aspects of verification related to on-chip communication between devices. First, the connectivity between masters and slaves, or masters, slaves and the interconnect network. Second aspect is the memory mapped registers being the ways of configuring and monitoring devices. The thesis document focuses on formal verification of System-on-Chip connectivity and register specification, and proposes new methodologies for extracting or completing the specifications where it is commonly and practically unavailable.

Thesis Summary

Reuse and integration of devices on a single chip are the main characteristics of the process of System-on-Chip design. The design process is mostly automated which makes it easier but more error prone, because it depends on user manually written specification and a lot of scripts and different tools. A part of the functional verification of the System-on-Chip design is concerned with verifying such input specification and its compliance with the System-on-Chip register transfer level code.

In this thesis we focus on verifying the specification of two aspects of System-on-Chip communication, namely the System-on-Chip interconnect and the memory mapped registers. We use formal assertion based verification because it gives more controllability and observability as compared to the conventional simulation techniques.

We also provide new approaches for inferring missing information in the user entered specification. For register specification we propose a methodology based on formal and System Verilog assertions to extract the hardware signal name corresponding to the logical register in memory mapped registers specification. And for verification engineers interested in doing formal verification for the System-on-Chip connectivity without having the interconnect specification, we propose two methodologies for inferring a comma separated values file describing the System-on-Chip interconnect based on standard System-on-Chip documentation or an incomplete or a previous version of the System-on-Chip register transfer level code.

The thesis is divided into six chapters as listed below:

Chapter 1:

It gives an introduction, background and the motivation behind the research.

Chapter 2:

This chapter discusses in brief what the System-on-Chip design is, and shows the challenges that both a design and a verification engineer encounter.

Chapter 3:

This chapter gives a brief overview about the assertions based verification and specifically explains the System Verilog Assertions language, and focuses on what is needed to cover for the course of this thesis work.

Chapter 4:

This chapter covers in brief the formal verification theories and the different formal algorithms and engines available today.

Chapter 5:

This chapter explains the so-called memory mapped registers found on devices on the System-on-Chip. The chapter shows what it takes to verify the register specification in simulation and in formal, shows that it is more efficient and easier done in formal. In this chapter we propose a new methodology based on using formal and System Verilog assertions to find a usually un-available information in the register specification that is necessary to enable complete verification of the register access policies.

Chapter 6:

This chapter talks about the second aspect of communication on the System-on-Chip which is connectivity between design modules. The chapter covers three areas of connectivity verification namely, System-on-Chip fabric verification in simulation, formal verification of connectivity specification, and the verification of secure paths on the chip. This chapter also introduces two methodologies for extracting connectivity specification where the verification engineer has no such specification, and that makes running formal connectivity verification easier and even possible.

Chapter 7:

Concluding the thesis and showing how to author verification plans for connectivity and register specification. Also in this chapter we discuss the potential future work.

Keywords:
Backdoor access, Bus interface, Connectivity, Formal Verification, Integration, IP Reuse, , IP-XACT, Memory Mapped Registers, System-on-Chip

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