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Abd-El Rahman Mohamed Ali Hassan El-Akhdar

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Ain Shams University, 2012

Supervisors

Prof. Dr. / Hadia Mohamed El-Hennawy

Prof. Dr. / Ayman Mohamed El-Tager

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Examiners' Committee

Name: **Abd-El Rahman Mohamed Ali Hassan El-Akhdar**
Thesis: High Power Microwave Applications
Degree: Doctor of Philosophy in Electrical Engineering

Title, Name and Affiliation	Signature
Prof. Dr./ Tamer Mostafa Abuelfadl Cairo University, Faculty of Engineering, Electronics and Electrical communications Dept.
Prof. Dr./ Hani Amin Ghali Ain Shams University, Faculty of Engineering, Electronics and Communications Engineering Dept.
Prof. Dr./ Hadia Mohamed El-Hennawy Ain Shams University, Faculty of Engineering, Electronics and Communications Engineering Dept.
Prof. Dr./ Ayman Mohamed El-Tager Military Technical College Electronics Engineering Dept.

Date:

STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Doctor of Philosophy in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

Name: Abd-El Rahman Mohamed Ali Hassan El-Akhdar

Signature:

Date:

Curriculum Vitae

Name of Researcher	Abd-El Rahman Mohamed El-Akhdar
Date of Birth	18/8/1981
Place of Birth	Egypt
First University Degree	B.Sc. in Electrical Engineering
Name of University	Military Technical College
Date of Degree	June 2003

List of publications:

- [1] **A. M. El-Akhdar**, H. M. El-Hennawy, and A. M. El-Tager, “**A Study on Double Via Row Configuration for SIW Based Structures,**” IEEE- International Conference on Microelectronics (ICM2016). 17-20 December 2016. Pp. 77-80.
- [2] **A. M. El-Akhdar**, A. M. El-Tager, and H. M. El-Hennawy, “**Investigation on Leakage Loss in Multiple Via Row SIW Structures,**” International Journal of Scientific & Engineering Research, Volume 8, Issue 3, March 2017. ISSN 2229-5518.
- [3] **A. M. El-Akhdar**, A. M. El-Tager, and H. M. El-Hennawy, “**Modeling of Double Via Row Configuration to Design SIW/HMSIW power Dividers/Combiners.**” Submitted to Journal of Electromagnetic Waves and Applications (JEMWA).
- [4] **A. M. El-Akhdar**, A. M. El-Tager, and H. M. El-Hennawy, “**Design and Modelling of Double Via Row Substrate Integrated Waveguides to Improve Bandwidth, Insertion Loss and Power Handling.**” Submitted to Special Issue of IEEE Transactions on Microwave Theory and Techniques.

ABSTRACT

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Key words: Substrate Integrated Waveguides, Double Via Row, High Power Circuits, Power dividers/combiners.

Substrate Integrated Waveguide (SIW) power dividers/combiners play an important role in modern 5G communication systems and millimetric wave applications. This thesis presents the development of SIW transmission lines using double via rows configuration to improve its power handling capability, operational bandwidth and to reduce its radiation loss. A model to calculate the effective width in double via row (DVR) structures is presented based on transmission line theory. Moreover, a graphical user interface (GUI) calculator program using MATLAB is proposed to help the designer to calculate SIW electrical parameters and obtain generalized design curves. The proposed model is verified through parametric analysis, fabrication and measurement of case studies using various design parameters. It is concluded that the best configuration using DVR SIW structure by using separation between vias equals to two times the via diameter and the distance between the parallel rows equals to three times the via diameter. The fabricated structure achieves 40% enhancement in insertion loss and 31.32% wider bandwidth and 42.85 % lower radiation loss compared to SIW structures utilizing single via row (SVR) configuration. A high-power measurement setup is applied to predict the power handling capability of the proposed structure.

The proposed structure based on the preferred design parameters is used to design SIW/HMSIW power divider/combiner with improved bandwidth and enhanced power handling capability. The fabricated DVR SIW/HMSIW power divider/combiner features good input/output matching, insertion losses and isolation between output ports. All measurements agree well with 3D EM simulations which verifies the proposed technique. Finally, the proposed DVR SIW achieves 16% smaller size, 30% wider bandwidth and better S-parameters than similar published work. The presented power divider/combiner is very promising in power amplifier design by combining multiple power transistors in both RF board level and LTCC package level.

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