Ain Shams University
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# Implementation of Parallel Digital Signal Processing Circuits using Field Programmable Gate Array

*A thesis submitted for the degree of Master of Science As a partial fulfillment of the requirements of the of Master of Science*

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# Abstract

The Compact Muon Solenoid (CMS) is one of the particle detectors based at CERN (The European Organization for Nuclear Research) designed to see a wide range of particles and phenomena produced in high-energy collisions at the Large Hadron Collider (LHC). It consists of many layers of detectors measure the different particles.

The CMS Muon system (lies at the end cap of the detector) has three types of gaseous detection technologies: Drift Tube Chambers (DTs), cathode strip chambers (CSCs), Resistive Plate Chambers (RPCs) and the new upgrade Gas Electron Multiplier (GEM).

This thesis is concerned with the digital readout electronics of the GEM detector where a specific algorithm has been designed and implemented using Field Programmable Gate Array (FPGA) device for processing (partitioning, zero suppression and multiplexing) signals generated from the GEM electronic board. Such a processed signal is then analyzed by feeding it as an input to a data acquisition system (DAQ).

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