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Equalization for High Speed Serial Data Transimission

A Thesis

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Abstract

This thesis studies equalization techniques for high speed serial data transmission. It presents the design of a Decision Feedback Equalizer (DFE) both at the system and circuit levels. The target application is serializer/deserializer (SERDES) working at a data rate of 10 Gb/s.

A Decision feedback equalizer using half-rate architectures is used. Half-rate architectures relax the requirements on the buffers speed and the clock skew, since consequent latches work at two different edges of the clock. The system uses 5 taps; this number of taps is found to be optimum. Increasing the number of taps enable the system to remove more ISI components. However, it increases the load on the summation circuit and the capacitance due to routing, which limits the performance. An adaptive least mean square (LMS) algorithm is used for tap coefficient calculation. The system doesn't use any speculation techniques; speculation techniques decrease the requirements on the slicer delay which enables the system to work at higher speeds. However, it increases area and power consumption of the system. It also increases the load, and complicates the design of other receiver blocks like the clock data recovery (CDR). New fast slicer architecture is introduced to enable 10Gb/s speed without speculation. This new architecture has higher speed and better sensitivity; however it consumes larger area and power than the conventional buffer used for other taps. The multiplication function of DFE system is achieved by a multiplying digital-to-analog converter (MDAC). The input (un-equalized signal) is applied to a differential pair, with degeneration resistor to increase its linearity, and degeneration capacitor to introduce some high frequency boosting at high frequency. Combining these functionalities into one block decreases the overall delay and so improves the system performance.

The decision feedback equalizer (DFE) system is designed in a 90-nm CMOS technology. This design consumes a power of 43mW from 1.2 supply voltage, and area of 177umX146um. Removing speculation improves power consumption by 60%. Five test cases for different transmission channel characteristics have been simulated as a test vehicle. The equalizer is shown to compensate for channel losses up to 22dB and achieve error-free data recovery.

Key words: Equalization techniques, Decision feedback equalization, High speed buffer design, Multiplying digital to analog converter, Summation Circuits.

Contents

List of Figures

List of symbols and abbreviations

ADC	Analog to Digital Converter
ADM	add/drop multiplexer
ANSI	American National Standards Institute
BER	Bit Error Rate
BW	BandWidth
CDR	Clock Data Recovery
CML	Current Mode Logic
CMU	Clock Multiplication Unit
CTF	Continuous Time Filter
DAC	Digital to Analog Converter
DFE	Decision Feedback Equalizer
DFF	Delay Flip Flop
DMUX	Dmultiplexer
ECSA	Exchange Carriers Standards Association
FFE	Feed-Forward Equalizer
FFT	Fast Fourier Transform
FIR	finite impulse response
FPD	Flat panel display
IC	Integrated Circuit