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**Equalization for High Speed Serial
Data Transimission**
A Thesis

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Abstract

This thesis studies equalization techniques for high speed serial data transmission. It presents the design of a Decision Feedback Equalizer (DFE) both at the system and circuit levels. The target application is serializer/deserializer (SERDES) working at a data rate of 10 Gb/s.

A Decision feedback equalizer using half-rate architectures is used. Half-rate architectures relax the requirements on the buffers speed and the clock skew, since consequent latches work at two different edges of the clock. The system uses 5 taps; this number of taps is found to be optimum. Increasing the number of taps enable the system to remove more ISI components. However, it increases the load on the summation circuit and the capacitance due to routing, which limits the performance. An adaptive least mean square (LMS) algorithm is used for tap coefficient calculation. The system doesn't use any speculation techniques; speculation techniques decrease the requirements on the slicer delay which enables the system to work at higher speeds. However, it increases area and power consumption of the system. It also increases the load, and complicates the design of other receiver blocks like the clock data recovery (CDR). New fast slicer architecture is introduced to enable 10Gb/s speed without speculation. This new architecture has higher speed and better sensitivity; however it consumes larger area and power than the conventional buffer used for other taps. The multiplication function of DFE system is achieved by a multiplying digital-to-analog converter (MDAC). The input (un-equalized signal) is applied to a differential pair, with degeneration resistor to increase its linearity, and degeneration capacitor to introduce some high frequency boosting at high frequency. Combining these functionalities into one block decreases the overall delay and so improves the system performance.

The decision feedback equalizer (DFE) system is designed in a 90-nm CMOS technology. This design consumes a power of 43mW from 1.2 supply voltage, and area of 177umX146um. Removing speculation improves power consumption by 60%. Five test cases for different transmission channel characteristics have been simulated as a test vehicle. The equalizer is shown to compensate for channel losses up to 22dB and achieve error-free data recovery.

Key words: Equalization techniques, Decision feedback equalization, High speed buffer design, Multiplying digital to analog converter, Summation Circuits.

Contents

List of figures	14
List of symbols and abbreviations	16
List of tables	17
1 Introduction to Serial Data Transmission	1
1.1 Introduction to SERDES	1
1.2 Applications	4
1.3 Backplane System	8
1.4 Eye Measurement Basics	10
1.5 Goals of the thesis	12
2 Equalization Theory and State of the Art	15
2.1 What is Equalization	15
2.2 Equalizer Types	15
2.3 Passive RLC high-pass Filter	20
2.4 Finite Impulse Response Filter	21
2.4.1 Traveling Wave Filter	23
2.4.2 Inductorless Analog Tap Delay Line	26
2.4.3 Fractionally Spaced FIR:	29

2.5	Transversal Filter	32
2.5.1	Serial Filter Combination	32
2.5.2	Parallel Filter Combination	37
2.6	Decision Feedback Equalizer	40
2.6.1	System Explanation	42
2.6.2	Tap Calculation Algorithm	42
2.6.3	Half Rate Architecture	43
2.6.4	Speculation	44
2.6.5	Decision Feedback Equalizer State of the Art	46
2.7	Summary	52
3	Decision Feedback Equalizer System Design	53
3.1	Introduction	53
3.2	System Design	54
3.3	DFE System Level Simulation	56
3.4	DFE System Testing	58
3.4.1	Case 1: 15" FR408 Backplane channel and bottom routed	61
3.4.2	Case 2: 25" FR408 Backplane channel and backdrilled	63
3.4.3	Case 3: 30" FR408 Backplane channel and backdrilled	65
3.4.4	Case 4: 15" FR408 Backplane channel and via stub	67
3.4.5	Case 5: Differential high-speed backplane	69
3.4.6	Summary	71
4	Decision Feedback Equalizer Circuit Design	73
4.1	Introduction	73
4.2	Latch Design	74
4.2.1	Buffer Design	74
4.2.2	Latch Topologies	76

<i>CONTENTS</i>	7
4.2.3 Latch Design	79
4.3 Slicer Design	83
4.4 Summation Circuit Design	89
4.5 Summary	95
5 Post Layout Simulation	97
5.1 Introduction	97
5.2 System Layout	97
5.3 Post Layout Simulation	100
5.4 Future Work	106
A Analysis of Decision Feedback Equalizer	107
B DFE Tap Calculation Algorithms	111
C Verilog-AMS Codes	115
D Speculation	119
References	121

List of Figures

1.1	Skew across a high-speed parallel bus limits the bandwidth of the bus.	2
1.2	Typical block diagram of a serial data communication system. . . .	3
1.3	Synchronous optical network (SONET) ring architecture based on a high-speed optical serial communication.	5
1.4	A parallel supercomputer grouping many computers linked by high-speed serial interconnections.	6
1.5	Various applications of the short-haul serial communication.	7
1.6	a. I-Trac 11 row Reference Backplane b. Daughtercard	8
1.7	Backplane channel characteristics. (a) Backplane/line card application. (b) Channel impulse response. (c) Channel frequency response.	9
1.8	Overlaying of bit sequences to form and eye diagram.	10
1.9	Eye Diagram parameters	11
1.10	Moving the BER decision point in time to trace out the BER profile of the crossing point.	12
2.1	Receiver Equalizers. a. Linear Equalizer b. Non Linear Equalizer .	18
2.2	Transversal Filter. a. Parallel combination b. Serial Combination .	19
2.3	Simple compensation networks (a) symmetric-T attenuator (b) by-passing is added (c) the network is duplicated for the complimentary signals IN- and OUT-	20
2.4	Sweep the time constants for the network	22
2.5	Sweep varying L2.	22

2.6	Functional block diagram of the FIR circuit.	23
2.7	conventional 3-tap FIR traveling wave filter (TWF) using artificial transmission lines.	24
2.8	The 3-tap FIR filter using a crossover TWF topology.	25
2.9	Distributed tap amplifier topologies. (a) Extending the crossover TWF topology to three or more amplifiers per tap resulting in asymmetric crossover routing. (b) The folded-cascade TWF makes use of an intermediate transmission line to perform the crossover routing with minimal delay mismatch.	25
2.10	A 3-tap folded-cascade TWF filter with programmable tap gains. .	26
2.11	Block diagram of six-tap FIR filter.	27
2.12	Delay cell half-circuit.	28
2.13	Gain stage.	28
2.14	Differential continuous-time analog tap delay unit using current-mode biquad.	30
2.15	INV-AIL delay cell.	31
2.16	Large-signal voltage transfer function of the INV-AIL delay cell. . .	31
2.17	a. Conventional filter stage b. its transfer function.	33
2.18	a. Filter stage with inductive peaking. b. its transfer function. . . .	33
2.19	Equalizer path with reverse scaling.	34
2.20	Equalizer feedback path	35
2.21	Modified Equalizing architecture.	36
2.22	Modified Equalizing filter stage.	36
2.23	(a) Spectrum decomposition. (b) Spectra of different compensation conditions.	37
2.24	Block diagram of conventional continuous-time adaptive cable equalizer.	38
2.25	Block diagram of conventional continuous-time adaptive cable equalizer.	40
2.26	Block diagram of new adaptive equalizer.	41

2.27	Magnitude plot of equalizer output for three different control voltages.	41
2.28	Decision Feedback Equalizer Block Diagram	42
2.29	Input data and half rate and full rate clock	43
2.30	Half Rate DFE system Block Diagram	44
2.31	DFE system Block Diagram with Speculation	45
2.32	Half Rate DFE system Block Diagram with Speculation	46
2.33	Receiver block diagram.	47
2.34	Circuit diagram of multiple-tap DFE summer.	47
2.35	Layout floorplans of odd DFE half. (a) Original floorplan. (b) Improved floorplan.	48
2.36	Receiver analog front end and DFE.	49
2.37	Transition sampling based CDR and DFE update. (a) and (b) CDR update. (c) and (d) DFE tap coefficients update.	51
2.38	Sense amplifier Schematic.	51
3.1	Decision Feedback Equalizer Block Diagram	54
3.2	Clock Signal and two bits of the input signal	57
3.3	channel characteristics	57
3.4	Eye diagram of input signal	58
3.5	Eye diagram of the equalized signal	59
3.6	Horizontal Eye Open versus DFF Delay	59
3.7	Convergence of tap weights	59
3.8	Channel Response. a. Molex Backplane b. Differential high-speed Backplane	60
3.9	Case 1 channel characteristics	61
3.10	Eye diagram of input signal for Case 1 channel	62
3.11	Eye diagram of the equalized signal for Case 1 channel	62
3.12	Tap weights convergence for Case 1 channel	62

3.13	Case 2 channel characteristics	63
3.14	Eye diagram of input signal for Case 2 channel	64
3.15	Eye diagram of the equalized signal for Case 2 channel	64
3.16	Tap weights convergence for Case 2 channel	64
3.17	Case 3 channel characteristics	65
3.18	Eye diagram of input signal for Case 3 channel	66
3.19	Eye diagram of the equalized signal for Case 3 channel	66
3.20	Tap weights convergence for Case 3 channel	66
3.21	Case 4 channel characteristics	67
3.22	Eye diagram of input signal for Case 4 channel	68
3.23	Eye diagram of the equalized signal for Case 4 channel	68
3.24	Tap weights convergence for Case 4 channel	68
3.25	Case 5 channel characteristics	69
3.26	Eye diagram of input signal for Case 5 channel	70
3.27	Eye diagram of the equalized signal for Case 5 channel	70
3.28	Tap weights convergence for Case 5 channel	70
3.29	Horizontal Eye Open Versus Tase Case number	71
3.30	Eye Amplitude Versus Tase Case number	72
4.1	(a) Neutralized CMOS differential pair. (b) Transfer characteristics.	75
4.2	Circuit schematic of a CMOS CML buffer.	77
4.3	Circuit schematic of a CMOS CML buffer 2	78
4.4	Circuit schematic of a CMOS CML buffer 3	78
4.5	Latch testbech	80
4.6	Simulation Results at TT, FF, SS corners	81
4.7	Latch Layout Design	82
4.8	Post Layout Simulation using SS corner	83

<i>LIST OF FIGURES</i>	13
4.9 New Latch topology	84
4.10 Slicer Simulation Results at TT, FF, SS corners	86
4.11 Amplifier Schematic	87
4.12 New and conventional latch delay versus input signal level	87
4.13 New Latch delay versus input signal level using Amplifier	88
4.14 New Latch Layout Design	88
4.15 New Latch post layout simulation	89
4.16 Summation circuit	90
4.17 Input transistors pair dc analysis	91
4.18 Input transistors pair gain	91
4.19 Current source (MDAC) simulation	93
4.20 Summation circuit simulation	94
4.21 Detailed Summation Circuit	95
5.1 System Layout Design	98
5.2 System Layout Design with annotations to the blocks	99
5.3 Case 1: Eye diagram of received signal	100
5.4 Case 1: Eye diagram of equalized signal	100
5.5 Case 2: Eye diagram of received signal	101
5.6 Case 2: Eye diagram of equalized signal	101
5.7 Case 3: Eye diagram of received signal	102
5.8 Case 3: Eye diagram of equalized signal	102
5.9 Case 4: Eye diagram of received signal	103
5.10 Case 4: Eye diagram of equalized signal	103
5.11 Case 5: Eye diagram of received signal	104
5.12 Case 5: Eye diagram of equalized signal	104
A.1 Decision Feedback Equalizer Block Diagram	107

B.1	Mean square error (MSE) surface	113
B.2	Error versus number of iteration at different μ	114
D.1	DFE system Block Diagram with Speculation	119
D.2	Half Rate DFE system Block Diagram	120

List of symbols and abbreviations

ADC	Analog to Digital Converter
ADM	add/drop multiplexer
ANSI	American National Standards Institute
BER	Bit Error Rate
BW	BandWidth
CDR	Clock Data Recovery
CML	Current Mode Logic
CMU	Clock Multiplication Unit
CTF	Continuous Time Filter
DAC	Digital to Analog Converter
DFE	Decision Feedback Equalizer
DFF	Delay Flip Flop
DMUX	Dmultiplexer
ECSA	Exchange Carriers Standards Association
FFE	Feed-Forward Equalizer
FFT	Fast Fourier Transform
FIR	finite impulse response
FPD	Flat panel display
IC	Integrated Circuit