



Ain Shams University
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Design of High Performance Pipelined ADC

A Thesis

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

Hussein Adel Hussein Ali, "Design of high performance pipelined ADC", Master of Science dissertation, Ain Shams University, 2010.

The thesis introduces calibration techniques as a method to achieve a high performance pipelined ADC with low power consumption. Digital calibration is suitable for the new sub-100nm technologies, as it benefits from the enhanced digital circuitry to relax the specifications of the analog circuits, which are impacted negatively by technology scaling.

To examine the extent of performance enhancement of the pipelined ADC due to digital calibration, two calibration techniques are proposed to calibrate an already designed ADC. The first one is a foreground technique which corrects for linear and non-linear errors. This technique does not require any modifications in the ADC, but it needs the ADC to be taken offline to perform calibration. The second technique is a concept validation for split ADC background calibration by using two identical versions of the designed ADC. This technique is efficient and works in the background while the ADC is online. However, it corrects for linear errors only.

Digital implementation is done on 65 nm technology for the foreground technique to examine the digital power and area overhead of the calibration technique.

Simulation results for the two proposed calibration techniques are presented, which show a significant enhancement in the ADC performance.

Key words: pipelined ADC, DEC, Linear Errors, Non-Linear Errors, Digital Calibration, Calibration Reference, Calibration Methodology, Input Forcing, Deterministic Approach, Statistical Approach, Split ADC

Summary

Chapter 1 includes thesis introduction and motivation for resorting to digital calibration techniques to design high performance ADCs in the new sub-100nm technologies. This chapter ends with the thesis outline..

Chapter 2 presents an overview of pipelined Analog-to-Digital Converters (ADC). Basic concepts such as sampling and quantization are explained along with definitions for a number of metrics used to characterize static and dynamic performance of ADCs. The pipelined ADC architecture is then presented with a discussion of the pipelined stage non-idealities and their effect on the ADC transfer function.

Chapter 3 presents and classifies an up-to-date literature review of state-of-the-art calibration techniques for pipelined ADCs. Definitions of various classifications for calibration are presented along with an introduction to the calibration concept. A practical classification is then introduced which differentiates between the reference of calibration for error detection and its method of correction. A detailed explanation for different calibration schemes is presented.

Chapter 4 presents two techniques for calibrating an already existing pipelined ADC. The first technique is a foreground technique, while the second one is a concept validation for a background calibration technique using split ADC concept. A brief description of the proposed ADC test chip is presented which is prepared for laboratory measurements. Distortion due to the reduced open loop gain of the residue amplifier is discussed.

Chapter 5 presents the digital implementation of the proposed foreground calibration. Area and power of the synthesized digital implementation are reported. Simulation results for the two proposed calibration techniques are presented.

The thesis ends by conclusions and future work.

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