AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications Engineering Department

Design of Building Blocks for H.264/AVC Video CODEC

A thesis submitted in partial fulfillment of the requirement of the Degree of Master of Science in Electrical Engineering

Submitted by

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STATEMENT

This thesis is submitted as partial fulfillment of the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering), Faculty of Engineering, Ain Shams University.

The work included in this thesis was carried out by the author in the department of Electronics and Communications Engineering, Ain Shams University.

No part of this dissertation has been submitted for a degree or a qualification at any other university or institute.

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Abstract

Design of Building Blocks for H.264/AVC Video CODEC

There is no doubt that the process of compressing video files while maintaining the quality and clarity of the image has become a very important issue because of the continuous increase in both of the size and quality of video files. Therefore, it is very important to use the standard systems in this field. These systems are constantly evolving through developing new methods for the processing of the video files to improve the compression efficiency than the previous ones.

H.264/AVC (Advanced Video Coding) is a relatively new industry standard for video compression. It is also known as MPEG-4 Part 10 and is a successor to earlier standards such as MPEG-2 and MPEG-4. It offers the potential for better compression efficiency (i.e. better-quality compressed video) and greater flexibility in compressing, transmitting and storing video. In this research, we will focus on design and implementation of some of the building blocks for this standard on FPGA.

The thesis starts with the study of H.264/AVC Video CODEC as an industry standard for video coding with its main features and applications. Then, the building blocks of the CODEC are studied. The building blocks of "inter prediction" process are selected to be designed and implemented, through which the motion estimation is performed on the non-overlapped Macro Blocks (MBs) forming the current frame to find the best match MBs in the reference frame. The resulting predicted frame is subtracted from the current frame to form the motion compensated residual frame.

Several Algorithms of the motion estimation process are then studied. The building blocks for the motion estimation using Three Step Search (TSS) algorithm and motion compensated residual frame calculation are implemented in "Verilog". The design includes the segmentation of the QCIF current frame into the 16x16 pixels non-overlapped MBs through a proper addressing of the memory locations of the pixels forming each MB.

The proposed design is implemented in “Verilog”, simulated using “ModelSim SE 6.3a”, synthesized using “Xilinx ISE Design Suite 12.4” and verified using “Excel”, ”MATLAB” and its add-on “SIMULINK”.

The thesis contains five chapters as follows:

- Chapter 1 presents the introduction to the digital video systems, video compression and general idea about CODEC.
- Chapter 2 explains H.264/AVC Video CODEC and its main features. The different building blocks are also explained.
- Chapter 3 focuses on Motion Estimation process and its different Algorithms.
- Chapter 4 has the full details of the design of the building blocks performing the inter prediction process. Both of the simulation results using “ModelSim SE 6.3a” and the synthesis results using “Xilinx ISE Design Suite 12.4” are presented. The simulation results are verified using “Excel”, ”MATLAB” and its add-on “SIMULINK”.
- Chapter 5 includes the conclusions and future work.

Finally, the thesis ends by a list of the references besides Appendix of ”Verilog" code of the developed design as well as Appendix of ”MATLAB" code for the design verification.

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List of Abbreviations

ASO	Arbitrary Slice Order
AVC	Advanced Video CODEC
BMA	Block matching Algorithm
BR	Bit Rate
CABAC	Context-based Adaptive Binary Arithmetic Coding
CAVLC	Context-based Adaptive Variable Length Coding
CB	Current macroBlock
CBDS	Center-Biased Diamond Search
CBP	Coded Block Pattern
CCIR	International Consultative Committee for Radio
CCITT	International Telegraph and Telephone Consultative Committee
CF	Current Frame
CIF	Common Intermediate Format
CLB	Configurable Logic Blocks
DCT	Discrete Cosine Transform
DS	Diamond Search
DVD	Digital Versatile Disk
EPZS	Enhanced Predictive Zonal Search
ExpG	Exponential-Golomb
FFS	Fast Full search
FMO	Flexible Macroblock Order
FPGA	Field Programmable Gate Array
FS	Full Search
HDSP	Horizontal Diamond Search Pattern
HVS	Human Visual System
IEC	International Electro-technical Commission
Intr	Interlaced
ISO	International Organization for Standardization
ITU-R	International Telecommunications Union-Radio Sector
ITU-T	International Telecommunications Union-Telecommunication Standardization Sector
JVT	Joint Video Team
LDSP	Large Diamond Search Pattern
LUT	Look Up Table
MAD	Mean of Absolute Differences
MAE	Mean Absolute Error