A Low-Power High-Speed ADC-Based Equalizer for Serial Links

by

Mostafa M. Ayesh
B.Sc. of Electrical Engineering
(Electronics and Communications Engineering)
Alexandria University, 2013

A thesis submitted in partial fulfillment of the
requirements for the degree of Master of Science in Electrical Engineering
Ain Shams University, Cairo

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AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

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Date: 22 / 5 / 2017

Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Thesis title: "A Low-Power High-Speed ADC-Based Equalizer for Serial Links"
Degree: Masters of Science in Electrical Engineering

Summary

The thesis is divided into six chapters including lists of contents, tables, and figures as well as a list of references.

Chapter 1
This chapter is an introduction including the motivation for this work, followed by the thesis outline.

Chapter 2
This chapter includes the literature survey for the analog and digital wireline receivers, and the literature survey for the high-speed ADCs.

Chapter 3
It describes the charge-steering concept, the circuit level of the proposed comparator, the proposed ADC and the overall system of the digital receiver.

Chapter 4
The chapter shows the system level and circuit level simulations. This chapter includes different results for schematics, post-layout simulations, and layouts.

Chapter 5
This chapter discusses the concept of equalization and the different types of equalization. It also provides a literature review for the equalizers and shows the designed DTLE along with its simulation results.

Chapter 6
This last chapter includes the conclusion for this work and the suggested future work on this system either an optimization or further needed implementation.

Thesis supervisors' signature

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Abstract

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Driven by an accelerating high demand in the interface IPs market for much faster communication links, market enormously moved from the parallel I/Os to high-speed serial links. An increasing hunger for more bandwidth appeared in all applications from networking and computers to wireless and consumer Electronic devices. Moreover, the end user has a growing need for faster exchange of data through Internet, watching full HD movies or listening to ultra-pure music using portable devices which should run for enough long time.

Multi-Gbps transceivers are expected to operate error-free for high-performance-based applications, consume as small silicon area and as low power as possible. This imposes new design and optimization challenges that are difficult to meet, especially for a small area, a low power, and a high speed. However, having a single PHY that meets multiple standards reduces the time-to-market of SOC designs. That is why large companies race to build their own multi-standard reconfigurable PHYs for new high data-rates and technology nodes.

One way to meet different standards is reconfigurability, heavily depending on programmability and the digital portion of the system. To make system easily reconfigurable we should process the signal digitally as much as we can, that is why ADC-based-receivers come ahead. ADC is utilized to change the signal from the analog domain to the digital domain where we can perform feed-forward equalization or decision-feed-back equalization with a variable number of switchable taps to achieve various ranges of channel equalization and hence meets multi-standard requirements.

The main challenge of the digital receivers is the ADC itself. To get high-data-rates, ADCs are required to be Flash to reach such speeds. Flash architectures are well-known traditionally to have the highest speeds, largest area and highest power dissipation.

This thesis proposes a 20-GS/s low-power ADC-based equalizer for high-speed serial wireline receivers. Digital receivers are recently adopted to overcome the challenges facing circuits in the analog domain such as power, delay, and mismatches, besides exploiting benefits of the digital circuits and systems, these benefits are scaling, different and easier adaptation algorithms, calibration, reconfigurability and noise immunity. The ADC-based

equalizer is designed and post-layout-simulated in a 65-nm CMOS technology. It consumes 15.5 mW in the ADC and 0.57 mW in the discrete-time linear equalizer from a 1-V and 1.2-V power supplies. Low power consumption is achieved by using time-interleaving in the ADC architecture, utilizing charge-steering concept, sharing single reference ladder across the four interleaved channels of ADC, and introducing a novel proposed design for the comparator itself in the Flash analog to digital converter besides using the novel discrete-time linear equalizer circuit.

Keywords: Flash ADC, Charge-Steering, High-speed ADC, Preamplifier, Linear Equalizers, Time-interleaved, ADC-based Equalizer, DTLE.

Publications: M. M. Ayesh, S. A. Ibrahim, H. F. Ragai, and M. M. Rizk “A Low-power High-speed Charge-steering ADC-based Equalizer for Serial Links,” ICECS, M.Sc/Ph.D. Forum, December 2015.

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"In a memoriam of my beloved passed-away-brother Eng. Mohamed Mahmoud Abdelkader Hassan, the Teaching Assistant at Mechanical Engineering Department-Alexandria University, who inspired me all the way after the high school".

M. Ayesh
May 2017

To my Father, my Mother, and my lovely wife Marwa

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