Ain Shams University
Faculty of Engineering
Electronics and Communications Engineering Department

Layout Proximity Effects for Analog Design

A Thesis
Submitted in proposing manual and automated flows for current mismatch calculation due to **STI** in layout of analog designs such as current mirrors circuits of a Master of Science degree in Electrical Engineering

Submitted by:
Inas Mohammed Mustafa Mohammed Abou-el-Seoud
B.Sc. of Electrical Engineering
(Electronics and Communications Engineering Department)
Ain Shams University, 2011.

Supervised by:
Prof. Dr. Mohamed Amin Dessouky
Dr. Hazem Said Ahmed

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Submitted by : Inas Mohammed Mustafa Mohammed Abou-el-Seoud

Thesis Title : **"Layout Proximity Effects for Analog Design"**

Degree : Master of Science in Electrical Engineering

Department : Electronics and Communications Engineering Dept.

Examiners' Committee

Prof. Dr. El-Sayed Mostafa Saad **……**

Helwan University

Faculty of Engineering

Electronics and Communications Engineering Department.

Prof. Dr. Hani Fikry Ragai **……**

Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department.

Prof. Dr. Mohamed Amin Dessouky **……**

Helwan University

Faculty of Engineering

Electronics and Communications Dept.

Defense Date:

Master of Science in Electrical Engineering

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Prof. Dr. Mohamed Dessouky

Ain Shams University

Faculty of Engineering

Electronics and Communication Engineering Dept.

Dr. Hazem Said Ahmed

Ain Shams University

Faculty of Engineering

Computer and Systems Engineering Dept.

Curriculum Vitae

Name:	Inas Mohammed Mustafa Mohammed Abou-el-Seoud
Date of Birth:	1/5/1989
Place of Birth:	Cairo, Egypt
First University Degree:	B.Sc. in Electrical Engineering
Name of University:	Ain Shams University
Date of Degree:	June 2011
Current Job:	Electrical Engineer
e-mail:	inasmostafa89@hotmail.com
	inasmostafa89@gmail.com
Signature:	
Date:	

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ABSTRACT

This thesis aims at introducing a proposed automatic flow for mitigating Layout Dependent Effect **"LDE"**. Among the **LDE** effects appearing in deep submicron technologies there is an important **LDE** effect called **Shallow Trench Isolation (STI)**. These effects can't be seen explicitly in the **PEX** and post layout simulations but only a change in circuit behavior can be deduced as a result from these effects. So in order to see these effects the chip needs to be fabricated then doing some measurements to judge correctly what the reason for the problem in this chip is. This also due to the fact of not having solid models for these effects, but all the efforts done in this field depend on some observations and developing empirical equations.

Analog layout is an exhausting and time consuming task, so several analog layout automation techniques have been invented to shorten the time to market like what is happening in the digital side in which all the flow is done in an automatic way. Each invented automatic technique is created to automate a certain stage in the analog layout flow, this is because there are several specifications need to be satisfied in the layout in order to be functional with its design, so there is no complete analog layout automation technique has been reached yet until this moment. Hence each analog layout automation tool technique in the market is targeting certain stage taking into considerations the difficulties and challenges exist in this stage.

The proposed automation flow presented in this thesis work won't automate a step in the analog layout flow but will propose a methodology by which the effect of the **STI** can be predicted earlier on the layout behavior against its design, since the fact that **LDE** effects mainly depend on the layout parameters. The **STI** effect will be examined for each sub-block forming the main circuit. By following this methodology

an optimal layout against **STI** effect for each sub-block is reached, which will guarantee a better functionality for the whole circuit after integrating these individual optimal layouts for each sub-block. The main circuits examples on which the effect of the **STI** appears clearly are the circuits containing matched devices. Hence these devices need special treatment in developing their layout such as making them have the same surrounding environment, try to have the same stress effect on each device, distribute them in a common-centroid configuration, and try as much as possible to get them far away from the stress edges.

As examples for circuits having matched devices are: **current mirrors**, and **differential pairs**. Thesis work will focus on current mirrors circuit type, this will be shown in the study for an **OTA** circuit against **STI** effect as a first case study. Then another bigger **NMOS** current mirror example will be used to develop the proposed automation flow. Since this circuit is a big one, it will have more than one pattern distribution to be studied, the target is to find the optimal distribution which will give the smallest mismatch between $\mathbf{I_{DS}}$ values after layout compared to the schematic values. But instead of doing the layout for each distribution then go through the whole manual layout design flow which will take much time, some changes will be done for each of the layout, schematic and test-bench to automate this flow. So that to have at the end an automatic flow takes any pattern distribution for this **NMOS** current mirror as an input then calculation for $\mathbf{I_{DS}}$ mismatch due to **STI** will take place, then select the optimal layout which will give the best results.

By this methodology of predicting the **STI** effect on each part of the design in an earlier stage, huge portion of time for post layout iterations is saved, in addition to have step by step communication between the design and layout.

Keywords: **LDE, STI, WPE, LOD, PSE, OSE, mobility, OTA, DRC, LVS, PEX.**

SUMMARY

Faculty of Engineering – Ain Shams University
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Layout Dependent Effects **(LDE)** is a new guest introduced with the frequent scaling down for the technologies starting from **65nm** technology process till it reaches to **28nm** and even smaller technology nodes. Analog design flow starts with having some specifications for which a design to be developed, after developing the design for a certain application, the next step is introduced, which is the layout generation step. In this step some information need to be taken into consideration as guidelines form the design perspective in order to help in generating a functional layout fulfilling most of the specifications too.

Then the post layout verifications started such as **DRC**, **LVS** and **Antenna**. Then **PEX** and **back annotation** is performed to check the functionality of the layout with its design. According to the results from the back annotation step, the validity of the layout will be determined, whether it needs some modifications or send it to the **FAB**. After the fabrication it is exposed to many types of testing which can reveal the effects that weren't appearing in the circuit simulations. But these effects definitely have reasons in the layout which can be avoided by the appropriate layout configurations. Among these effects is the **STI** effect which will be the focus for this thesis work. This effect will be studied using two proposed flows: **manual flow using an OTA circuit for study**, and **automatic flow using NMOS current mirror circuit**

for developing this flow. By this methodology, a proposed automatic flow is created by which the **STI** effect can be predicted for each sub-block forming the main circuit under study.

Accordingly, the thesis is organized in six chapters as follows:

Chapter 1: Includes a brief introduction about the motivation, thesis contributions and organization.

Chapter 2: Introduces a background about the different layout dependent effects and the reason of their appearance especially in the nanometer technology nodes.

Chapter 3: Presenting the earlier efforts done in the field of modeling these layout dependent effects, in addition of making use of them in enhancing some circuits performance as will be shown for standard cells used in the digital designs.

Chapter 4: Introduces the thesis actual work which is the **STI mitigation** and exploring different methodologies for doing that, then finally reaching to an automated approach for doing this on variety of current mirror layout distributions.

Chapter 5: Integrating the **STI mitigation** flow with the **genetic optimizer** and show the results of this integration again on the same example of the current mirror will be shown in this chapter.

Chapter 6: Shows the conclusion and proposed future work in the same field of the analog automation flow. Proposing some ideas for enhancing the flow more and more to be fully automated without the need of any manual interference. Also adding some techniques which will help in providing more information about the layout effect on the design in early phases of the design.

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