بسم الله الرحمن الرحيم

شبكة المعلومـــــات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكروفيلم

﴿ قـــسـم ﴾

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأفلام قد اعدت دون آية تغيرات

يجب أن

تحفظ هذه الأفلام بعيداً عن الغبار

في درجة حرارة من 15 – 20 مئوية ورطوبة نسبية من 20-40 %

To be kept away from dust in dry cool place of
15 – 25c and relative humidity 20-40 %

بعض الوثائق الأصلية تالفة

بالرسالة صفحات

لم ترد بالأصـــل

Ain Shams University
Faculty of Engineering
Electronics and Communicayion Eng. Dept.

New Full-Voltage-Swing Multi-Drain/Multi-Collector Complementary BiCMOS Buffers (M^2 CBiCMOS)

Submitted By
Mohammed M. El-Hady Attya
M.Sc. in Electrical Engineering

A THESIS

Submitted In Partial Fulfillment for the Requirements of the Degree Of Ph.D. In Electrical Engineering
Electronics and Communicayion Engineering Department

Supervised by

Prof. Dr. M. H. Elsaid
Dr. H. Haddara

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Ph.D. in Electronics and Computer Engineering.

The work included in this thesis was carried out by the author in the department of Electronics and Computer, Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other university or institution.

Date : May, 1998

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Abstract

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In this thesis, we introduce novel circuit techniques, based on transiently saturating the BJTs using a base current pulse, for increasing the voltage swing of BiCMOS buffers. These circuit techniques employ multi-drain MOS's and/or multi-collector BJTs structures.

The reduction in the effective gate voltage of the MOSFET device of conventional BiCMOS circuit has been improved using a modified BiCMOS (MBiCMOS) circuit configuration. This MBiCMOS circuit improves the speed performance of conventional BiCMOS circuit at reduced supply voltages (3 V). However, it does not assure full-voltage-swing operation. Moreover, the speed performance and circuit complexity of the common emitter CBiCMOS circuits have been improved employing a new modified CBiCMOS (MCBiCMOS) buffer. This new circuit employs multi-drain BiCMOS structure to isolate the bases of the employed BJTs, reduce the BJTs turn-off time and improve the speed performance with no additional circuit complexity (reduce the number of discrete components per gate). The MCBiCMOS circuit offers full-voltage-swing operation and high speed performance for reduced supply voltages (2.5 V). However, it suffers from increased process complexity (fabrication of high performance *pnp* BJTs).

The aim of this work is to introduce three novel implementations of CBiCMOS buffers (CBiCMOS-A, CBiCMOS-B and CBiCMOS-C). These circuits employ multi-drain/ multi-collector CBiCMOS structure. The new circuits are configured so that the *pnp* BJTs are implemented only in the internal parts of the circuits, while the output drivers employ *npn* BJTs. In this case, the effect of the collector resistance R_{cp} of the *pnp* BJT's is negligibly small compared to the effect of the collector resistance R_{cn} of the *npn* BJT's on the propagation delay-time. This allows the implementation of non-optimized *pnp* BJTs (employing lateral BJT in MOSFET structure) with no additional process complexity. The multi-drain/multi-collector structure is implemented in the CBiCMOS-B and CBiCMOS-C buffers to isolate the bases of the BJTs. This structure is necessary to reduce the BJTs turn-off time, ensure full-voltage-swing operation and improve speed performance at lower

supply voltage (less than 2V)). Furthermore, this multi-structure offers less circuit complexity (reduce the number of devices per gate) and area saving.

The transient behavior of the CBiCMOS-B is studied using analytical delay-time modeling. The presented modeling equations accounts for device parasitic and high injection effects of the implemented BJTs on the propagation delay-time.

In addition, an optimized circuit layout for the CBiCMOS-C driver, employing, multi-drain/multi-collector CBiCMOS structure, is presented. The introduced circuit layout ensures minimum chip area and optimized wire routing with minimized wire length, minimum number of crossovers and minimum number of interconnects (low cost/ high packing density), and low parasitic components values.

In this thesis, we present simulation results related to the new circuit configurations of the BiCMOS and CBiCMOS buffers. We demonstrate the effects of power supply voltages scaling, parasitic components and loading capacitance on the speed performance of the MBiCMOS, MCBiCMOS and the multi-drain/multi-collector CBiCMOS buffers (CBiCMOS-A, CBiCMOS-B and CBiCMOS-C). These effects are also compared with that of the conventional BiCMOS and CBiCMOS circuits. The effects of the parasitic components of the *pnp* BJTs on the speed performance are also introduced and compared to that of the *npn* BJT's. Simulation results show that implementation of non optimized lateral *pnp* BJT in MOSFET structure does not appreciably affect the speed performance of the proposed buffers. The analytical results are given and compared with the SPICE simulations to verify this analytical model.

Key Words

CBiCMOS Buffer- Simulation-DelayTime Modeling

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To: My Parents
My Wife
My Kids,
Sameh, Amer, and Marwa

M. M. El-Hady

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