

بسم الله الرحمن الرحيم





شبكة المعلومات الجامعية التوثيق الالكتروني والميكروفيلم



جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

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بعض الوثائق الأصلية تالفة





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FPGA Application in Digital Circuit

**Thesis Submitted in a Partial Fulfillment for the
Master of Science Degree In
Communications Eng.**

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Eng. Ahmed Mohamed Abd El-Gawad

DEDICATION

*Thanks to God who helped me to finish this research.
From my heart and my soul, I dedicate this work*

Especially to

My mother

My little baby

Salma

My wife

Ahmed M. Abd El-Gawad

List of Abbreviations

<i>ATE</i>	Automatic Test Equipment
<i>BIST</i>	Built In Self Test
<i>BUT</i>	Board Under Test
<i>CAD</i>	Computer-Aided Design
<i>CMOS</i>	Complementary Metal Oxide Semiconductor
<i>COTS</i>	Commercial Off The Shelf
<i>CUT</i>	Circuit Under Test
<i>DFT</i>	Design for Test
<i>DL</i>	Defect Level
<i>DRAM</i>	Dynamic RAM
<i>EDIF</i>	Electronic Design Interchange Format
<i>EPROM</i>	Erasable Programmable Read Only Memory
<i>EEPROM</i>	Electrical Erasable Programmable Read Only Memory
<i>FC</i>	Fault Coverage
<i>FPGA</i>	Field Programmable Gate Array
<i>FSM</i>	Finite State Machines
<i>IC</i>	Integrated Circuit
<i>ICT</i>	In-Circuit Testing
<i>LCD</i>	Liquid Crystal Displays
<i>LFSR</i>	Linear Feedback Shift Register
<i>LRU</i>	Line Replaceable Unit
<i>LSI</i>	Large Scale Integration
<i>MCM</i>	Multichip Module
<i>MISR</i>	Multiple Input Shift Register
<i>MSI</i>	Medium Scale Integration
<i>OEM</i>	Original Equipment Manufacturer
<i>PCB</i>	Printed Circuit Board
<i>PAL</i>	Programmable Array Logic
<i>PLD</i>	Programmable Logic Device
<i>PROM</i>	Programmable Read Only Memory
<i>RASSP</i>	Rapid Prototyping of Application Specific Signal Processors
<i>ROM</i>	Read Only Memory
<i>SOC</i>	System On Chip
<i>SRAM</i>	Static RAM
<i>SSA</i>	Single Stuck-at
<i>SSI</i>	Small Scale Integration
<i>TPS</i>	Test Program Set
<i>TTL</i>	Transistor Transistor Logic
<i>VHDL</i>	Very high speed integrated circuit Hardware Description Language
<i>VLSI</i>	Very Large Scale Integration
<i>Y</i>	Yield

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Summary

Increasing circuit complexity, higher performance and the demand for high quality levels is causing the industry to question currently used functional and specification based test programs. In addition, the escalating cost of production test equipment capable of measuring high performance device parameters is in many cases becoming a limiting factor.

Pseudorandom testing could be of value to digital circuits, since it does not need any effort in test generation. The pseudorandom testing methodology can also be easily applied to any class of boards under study, so we use this technique in our proposed system. In the proposed system the testing takes place as follow:

At first the Board Under Test (BUT) will simulated to get the signature of free fault circuit and all possible faults signatures. All signatures will be stored in the FPGA, which will contain also the testing system. The proposed system used to generate random pattern. This pattern will be access to the BUT. The response will access to the proposed system to compress it by using Multiple Input Shift Register (MISR) to get signature. The signature will be compared with all signatures stored to know if the BUT is fault free or faulty and what is the fault. The result will appear on an LCD.

In this thesis one chip (FPGA) is used to implement an automatic testing Equipment (ATE), implemented and tested successfully. An Altera Flex10k EPF10K20RC240 chip was used in the implementation.