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شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

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بعض الوثائق الأصلية تالفة

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Mansoura University
Faculty of Engineering
Electronics&Comm.Eng.Dep.

FPGA Application in Digital Circuit

Thesis Submitted in a Partial Fulfillment for the

Master of Science Degree In

Communications Eng.

By

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My Cardinal gratitude are dedicated to My Family

Eng.Ahmed Mohamed Abd El-Gawad

DEDICATION

Thanks to God who helped me to finish this research.
From my heart and my soul, I dedicate this work

Especially to

My mother

My little baby

Salma

My wife

Ahmed M. Abd El-Gawad

List of Abbreviations

ATE	Automatic Test Equipment
BIST	Built In Self Test
BUT	Board Under Test
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
CUT	Circuit Under Test
DFT	Design for Test
DL	Defect Level
DRAM	Dynamic RAM
EDIF	Electronic Design Interchange Format
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrical Erasable Programmable Read Only Memory
FC	Fault Coverage
FPGA	Field Programmable Gate Array
FSM	Finite State Machines
IC	Integrated Circuit
ICT	In-Circuit Testing
LCD	Liquid Crystal Displays
LFSR	Linear Feedback Shift Register
LRU	Line Replaceable Unit
LSI	Large Scale Integration
MCM	Multichip Module
MISR	Multiple Input Shift Register
MSI	Medium Scale Integration
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PAL	Programmable Array Logic
PLD	Programmable Logic Device
PROM	Programmable Read Only Memory
RASSP	Rapid Prototyping of Application Specific Signal Processors
ROM	Read Only Memory
SOC	System On Chip
SRAM	Static RAM
SSA	Single Stuck-at
SSI	Small Scale Integration
TPS	Test Program Set
TTL	Transistor Transistor Logic
VHDL	Very high speed integrated circuit Hardware Description Language
VLSI	Very Large Scale Integration
Y	Yield

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Summary

Increasing circuit complexity, higher performance and the demand for high quality levels is causing the industry to question currently used functional and specification based test programs. In addition, the escalating cost of production test equipment capable of measuring high performance device parameters is in many cases becoming a limiting factor.

Pseudorandom testing could be of value to digital circuits, since it does not need any effort in test generation. The pseudorandom testing methodology can also be easily applied to any class of boards under study, so we use this technique in our proposed system. In the proposed system the testing takes place as follow:

At first the Board Under Test (BUT) will simulated to get the signature of free fault circuit and all possible faults signatures. All signatures will be stored in the FPGA, which will contain also the testing system. The proposed system used to generate random pattern. This pattern will be access to the BUT. The response will access to the proposed system to compress it by using Multiple Input Shift Register (MISR) to get signature. The signature will be compared with all signatures stored to know if the BUT is fault free or faulty and what is the fault. The result will appear on an LCD.

In this thesis one chip (FPGA) is used to implement an automatic testing Equipment (ATE), implemented and tested successfully. An Altera Flex10k EPF10K20RC240 chip was used in the implementation.