AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Novel Frequency-Domain-Based Methodology for Signal Integrity

A Thesis submitted in partial fulfillment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

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Statement

This thesis is submitted as a partial fulfilment of Doctor of Philosophy in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Gordon Moore expected that the number of components will increase exponentially by the years. In agreement, the International Technology Roadmap for Semiconductors expects that the clock frequency will continue to increase while the feature size minimizes to smaller size. Despite that the performance of digital systems can be enhanced by improving several aspects including the increase of clock frequency, signal integrity effects begin to have a significant impact on system performance, which have been neglected at low frequencies. Therefore, these interconnect is no longer an ideal transparent wire and their behaviour that dependent on frequency will impact the propagation of signals by introducing glitches, delays and distortions. Historically, typical analysis of signal integrity problems, such as reflections, ringing, signal loss, distortion, delay, etc., is performed in time domain and so it cannot account for the elements with frequency-dependent behaviour in a direct way. Therefore, transforming signal and system specifications in the time domain to the frequency domain and performing the complete frequency-domain-based signal integrity analysis would simplify the process and make it more efficient, faster and more intuitive. The work presented in this thesis is to quantify the relationship between time domain aberrations of the clock signal and their frequency-domain characteristics. A point-to-point communication model is built on Keysight's Advanced Design System to justify these models.

Keywords: Clock Signal, Frequency Domain, High Frequency, Ringing, Signal Integrity, Time Domain.

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List of Abbreviations

ADS	**A**dvanced **D**esign **S**ystem
BUJ	**B**ounded-**U**ncorrelated **J**itter
CNT	**C**arbon **N**ano**T**ubes
DC	**D**irect **C**urrent
DCD	**D**uty-**C**ycle **D**istortion
DDJ	**D**ata **D**ependent **J**itter
DDR	**D**ouble **D**ata **R**ate synchronous dynamic random-access memory
DJ	**D**eterministic **J**itter
EMI	**E**lectromagnetic **I**nterference
FD	**F**requency **D**omain
FDTD	**F**inite-**D**ifference **T**ime **D**omain
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
HHT	**H**uang-**H**ibert **T**ransform
HT	**H**ibert **T**ransform
IBIS	**I**nput **B**uffer **I**nformation **S**pecification
ICs	**I**ntegrated **C**ircuits
IFFT	**I**nverse **F**ast-**F**ourier **T**ransform
IO	**I**nput **O**utput
ISI	**I**nter-**S**ymbol **I**nterference

ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductor
MIPS	**M**ega **I**nstruction **P**er **S**econd
MtM	**M**ore **t**han **M**oore
NRZ	**N**on **R**eturn to **Z**ero
OCT	**O**n-**C**hip **T**ermination
ODT	**O**n-**D**ie **T**ermination
PAM	**P**ulse **A**mplitude **M**odulation
PCB	**P**rinted **C**ircuit **B**oard
PDF	**P**robability **D**ensity **F**unction
PEEC	**P**artial **E**lement **E**quivalent **C**ircuit
PJ	**P**eriodic **J**itter
PSD	**P**ower **S**pectral **D**ensity
RC	**R**esistance-**C**apacitance
RCL	**R**esistance- **C**apacitance- **I**nductance
RJ	**R**andom **J**itter
SI	**S**ignal **I**ntegrity
SoC	**S**ystem **o**n **C**hip
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
STFT	**S**hort-**T**ime **F**ourier **T**ransform
TD	**T**ime **D**omain
TDFE	**T**ime **D**omain **F**inite **E**lement
TDR	**T**ime-**D**omain **R**eflectometer
TSMC	**T**aiwan **S**emiconductor **M**anufacturing **C**ompany
VHDL	**V**ery high-speed integrated circuit **H**ardware **D**escription **L**anguague
WT	**W**avelet **T**ransform