



AIN SHAMS UNIVERSITY  
FACULTY OF ENGINEERING  
Electronics Engineering and Electrical Communications

# Novel Frequency-Domain-Based Methodology for Signal Integrity

*A Thesis submitted in partial fulfillment of the requirements of  
the degree of*

Doctor of Philosophy in Electrical Engineering  
(Electronics Engineering and Electrical Communications )

by

Ahmed Saeed Abdelsamea Sayed

Master of Science in Electrical Engineering  
(Electronics Engineering and Electrical Communications )  
Faculty of Engineering, Helwan University, 2010

Supervised By

Prof. Hani Fikri Ragai  
Prof. Yehea Ismail Mohamed  
Assoc. Prof. Alaa Elrouby

Cairo - 2017



AIN SHAMS UNIVERSITY  
FACULTY OF ENGINEERING  
Electronics Engineering and Electrical Communications

**Name: Ahmed Saeed Abdelsamea Sayed**

# Novel Frequency-Domain-Based Methodology for Signal Integrity

**Degree: Doctor of Philosophy in Electrical Engineering**

## **Examiners' Committee**

<b>Name and Affiliation</b>	<b>Signature</b>
<b>Prof. Mohamed I. Eladawy</b> Electronics and Communications , Helwan University	.....
<b>Prof. Abdelhalim Abdelnaby Zekry</b> Electronics and Communications , Ainshams University	.....
<b>Prof. Hani Fikri Ragai</b> Electronics and Communications , Ainshams University	.....

## Statement

This thesis is submitted as a partial fulfilment of Doctor of Philosophy in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Ahmed Saeed Abdelsamea Sayed

Signature: .....

17 May 2017

## Researcher Data

Name : Ahmed Saeed Abdelsamea Sayed  
Date of birth : 21-09-1980  
Place of birth : Cairo  
Last academic degree : Master of Science in Electrical  
Engineering  
Field of specialization : Electronics and Communication  
University : Helwan University  
Date of issued degree : 2010  
Current job : Assistant Lecturer, Future  
University in Egypt

# Abstract

Gordon Moore expected that the number of components will increase exponentially by the years. In agreement, the International Technology Roadmap for Semiconductors expects that the clock frequency will continue to increase while the feature size minimizes to smaller size. Despite that the performance of digital systems can be enhanced by improving several aspects including the increase of clock frequency, signal integrity effects begin to have a significant impact on system performance, which have been neglected at low frequencies. Therefore, these interconnect is no longer an ideal transparent wire and their behaviour that dependent on frequency will impact the propagation of signals by introducing glitches, delays and distortions. Historically, typical analysis of signal integrity problems, such as reflections, ringing, signal loss, distortion, delay, etc., is performed in time domain and so it cannot account for the elements with frequency-dependent behaviour in a direct way. Therefore, transforming signal and system specifications in the time domain to the frequency domain and performing the complete frequency-domain-based signal integrity analysis would simplify the process and make it more efficient, faster and more intuitive. The work presented in this thesis is to quantify the relationship between time domain aberrations of the clock signal and their frequency-domain characteristics. A point-to-point communication model is built on Keysight's Advanced Design System to justify these models.

---

**Keywords:** Clock Signal, Frequency Domain, High Frequency, Ringing, Signal Integrity, Time Domain.

# Acknowledgment

Undoubtedly I owe to my advisers, Prof. Hani Fikri, Prof. Yehea Ismail and Prof. Alaa Elrouby a great deal. They have greatly supported me under every possible aspect of this long and difficult journey. They have been continuous source of motivation, and inspiration. They have provided guidance, technical criticism, valuable feedback. There is a fourth person, Prof. João Canas Ferreira (INESC TEC, Faculdade de Engenharia, Universidade do Porto, Porto, Portugal), that I truly feel I can address him as coadviser for this work. Two important contributions of this thesis have originated from a mobility program at Sistemas e arquitetura laboratório, DEEC, Faculdade de Engenharia, Universidade do Porto. Most importantly, the still ongoing interactions with Prof. Ferreira after that mobility have brought to my work both deep theoretical understanding as well as attention to practical implications.

I would like to thank the PhD jury members, Prof. Mohamed ELadawy (Helwan University), who has reviewed with overwhelming attention and criticism my thesis, and Prof. Abdelhaleem Zikry (Ainshams University), who has provided valuable feedback during my qualifying exam and during my dissertation talk. The discussion with Prof Mohamed Aboelatta (Ainshams University) was very helpful in both the scientific and administrative aspects. Hazim Ali (CISTER) and Mohamad Abdellatif (BUE) have contributed to this work with interactions and technical discussions through the mobility journey.



# Contents

<b>Statement</b>	<b>iii</b>
<b>Abstract</b>	<b>vii</b>
<b>Acknowledgements</b>	<b>xi</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Background . . . . .	1
1.2 Simulation techniques for Signal Integrity . . . . .	9
1.2.1 3D Field Solver . . . . .	9
1.2.2 Transmission-Line-Based Simulators . . . . .	11
1.3 Motivation . . . . .	12
1.4 Thesis Structure . . . . .	14
<b>2 Frequency-Domain Translation of Clock Signal</b>	<b>15</b>
2.1 Introduction . . . . .	15
2.2 Frequency Analysis Techniques . . . . .	16
2.3 Clock Signal Modeling . . . . .	20
2.3.1 The Ideal Clock . . . . .	21
2.3.2 Clock Skew . . . . .	23
Skew Definition . . . . .	23



Skew Modeling . . . . .	27
2.3.3 Clock Ringing . . . . .	31
Ringing Definition . . . . .	31
Ringing Modeling . . . . .	34
2.3.4 Rise and Fall time . . . . .	41
Rise/Fall Time Definition . . . . .	41
Rise/Fall Time Modeling . . . . .	43
2.3.5 Jitter . . . . .	47
Jitter Definition . . . . .	47
Jitter Modeling . . . . .	50
2.4 Summary . . . . .	60
<b>3 System Model and Verification</b>	<b>61</b>
3.1 Communication System: Interconnections Level . . . . .	61
3.1.1 Interconnect Model . . . . .	62
3.1.2 Sender and Receiver Model . . . . .	64
3.1.3 System Model and simulation setup . . . . .	66
3.2 Simulation Results . . . . .	69
3.3 Summary . . . . .	77
<b>4 Conclusions and Future Work</b>	<b>79</b>
4.1 Summary and Conclusions . . . . .	79
4.2 Suggestions for Future Work . . . . .	81

## List of Figures

1.1	TSMC Technology growth (Adapted from: <a href="http://www.tsmc.com">www.tsmc.com</a> )	2
1.2	CMOS scaling for "More than Moore". (Adapted from: <a href="http://www.iot.ieee.org">www.iot.ieee.org</a> )	3
1.3	Clock frequencies increase over the years. (Adapted from: [7])	4
1.4	Future computational power. (Adapted from: [8])	4
1.5	Measured response due to existence of through-hole via in uniform 38-cm-long trace in a 10-layers PCB. (Adapted from: [11])	5
1.6	100 MHz clock signal exhibit ringing due to impedance mismatch. (Adapted from: [11])	6
1.7	Signal integrity problems	7
1.8	Signal aberrations: ideal signal (blue), real world (red).	7
2.1	Ideal Clock Waveform	22
2.2	Ideal clock signal in the frequency domain: a) Magnitude spectra, b) Phase spectra.	24
2.3	Clock skew definition	25
2.4	Lead and lag skew definition	26

2.5	Clock signal and its skewed version for $A = 1.5$ : a) Synthesized signals from their Fourier series expansion, b) Magnitude spectra, c) Phase spectra. . . . .	28
2.6	Phase spectra of two signals with different values of skew: a) Wrapped phase, b) Unwrapped phase. . . . .	30
2.7	Ringing in clock signal. . . . .	33
2.8	Ideal and oscillating clock signals ( $\zeta=0.2$ and $f_n=1.4$ GHz): a) synthesized signals from their Fourier series expansion, b) Magnitude spectra, c) Phase spectra. . . . .	36
2.9	Effect of changing the parameters on phase spectrum: a) Different values of $f_n$ ( $\zeta=0.2$ , $f_o=200$ MHz), b) Different values of $f_o$ ( $\zeta=0.3$ , $f_n=1.8$ GHz), c) Different values of $\zeta$ ( $f_n=1.400$ GHz, $f_o=200$ MHz). . . . .	37
2.10	Same ratio of $f_n/f_o$ produces the same phase shape. . . . .	38
2.11	Relation between $ D_n $ , $\zeta$ and the ratio between $f_n$ and $f_o$ based on (2.23). . . . .	39
2.12	Trapizoidal approximation of the clock signal with unequal rise time $t_r$ and fall time $t_f$ . . . . .	42
2.13	response of first-order system to step input, illustrating the delay time, fall time and rise time. . . . .	43
2.14	Ideal and clock with rise and fall times signals ( $A = 1.5$ ): a) Synthesized signals from their Fourier series expansion, b) Magnitude spectra, c) Phase spectra. . . . .	45

2.15	Actual and jittered clock Signals. $J_{AC}$ is the time difference between jittered clock transition and ideal transition. . . . .	47
2.16	Jitter components. . . . .	48
2.17	Evaluation of the dual-Dirac PDF by convolving of the sum of two delta functions positioned at $\mu_L$ and $\mu_R$ and RJ represented by Gaussian distribution. . . . .	51
2.18	For small angle $\theta$ , the value of $\sin(\theta)$ can be reduced to $\theta$ while $\cos(\theta)$ reduced to 1. . . . .	53
2.19	Real and jittered clock signals ( $A = 1.5$ , $\sigma = 80\text{pS}$ ): a) Synthesized signals from their Fourier series expansion (up to the 7 <sup>th</sup> harmonic), b) Power Spectral Density of the real clock, c) Power Spectral Density of the jittered clock. . . . .	58
2.20	Probability density function of the generated jitter . . . . .	59
2.21	The value of random jitter used in the simulation . . . . .	59
3.1	A general communications system model. . . . .	61
3.2	Communication between two chips on the same PCB (adapted from [19]) . . . . .	62
3.3	IBM Supercomputer hierarchy (Source: [69]) . . . . .	63
3.4	Evolution of interconnect from lumped capacitor to distributed RC model, then, nowadays, distributed RCL model . . . . .	64
3.5	IBIS buffer models. a) Input buffer, b) output buffer (Source: [70]) . . . . .	65
3.6	System model and Simulation Setup . . . . .	67

3.7 Adding series resistor halfway between the driver and receiver to compensate the drop of the driver’s impedance . . 68

3.8 The effect of changing the series resistor in the overshoot and rise time (Source: [76]) . . . . . 69

3.9 200 MHz skewed signal: a) Signal obtained from ADS time-domain simulation, b) Magnitude spectrum, c) Phase spectrum. . . . . 71

3.10 100 MHz Oscillating clock signal obtained from circuit simulation: a) Signal, b) Magnitude spectrum, c) Phase spectrum. 73

3.11 100 MHz clock signal obtained from circuit simulation: a) Signal, b) Magnitude spectrum, c) Phase spectrum. . . . . 74

3.12 100 MHz jittered clock signal obtained from circuit simulation: time-domain signal. . . . . 75

3.13 100 MHz jittered clock signal obtained from circuit simulation: a) eye diagram, b) jitter histogram, c) Power Spectral Density of the jittered clock. . . . . 76

## List of Abbreviations

<b>ADS</b>	<b>Advanced Design System</b>
<b>BUJ</b>	<b>Bounded-Uncorrelated Jitter</b>
<b>CNT</b>	<b>Carbon NanoTubes</b>
<b>DC</b>	<b>Direct Current</b>
<b>DCD</b>	<b>Duty-Cycle Distortion</b>
<b>DDJ</b>	<b>Data Dependent Jitter</b>
<b>DDR</b>	<b>Double Data Rate synchronous dynamic random-access memory</b>
<b>DJ</b>	<b>Deterministic Jitter</b>
<b>EMI</b>	<b>Electromagnetic Interference</b>
<b>FD</b>	<b>Frequency Domain</b>
<b>FDTD</b>	<b>Finite-Difference Time Domain</b>
<b>FPGA</b>	<b>Field Programmable Gate Array</b>
<b>HHT</b>	<b>Huang-Hibert Transform</b>
<b>HT</b>	<b>Hibert Transform</b>
<b>IBIS</b>	<b>Input Buffer Information Specification</b>
<b>ICs</b>	<b>Integrated Circuits</b>
<b>IFFT</b>	<b>Inverse Fast-Fourier Transform</b>
<b>IO</b>	<b>Input Output</b>
<b>ISI</b>	<b>Inter-Symbol Interference</b>

<b>ITRS</b>	<b>I</b> nternational <b>T</b> echnology <b>R</b> oadmap for <b>S</b> emiconductor
<b>MIPS</b>	<b>M</b> ega <b>I</b> nstruction <b>P</b> er <b>S</b> econd
<b>MtM</b>	<b>M</b> ore than <b>M</b> oore
<b>NRZ</b>	<b>N</b> on <b>R</b> eturn to <b>Z</b> ero
<b>OCT</b>	<b>O</b> n- <b>C</b> hip <b>T</b> ermination
<b>ODT</b>	<b>O</b> n- <b>D</b> ie <b>T</b> ermination
<b>PAM</b>	<b>P</b> ulse <b>A</b> mplitude <b>M</b> odulation
<b>PCB</b>	<b>P</b> rinted <b>C</b> ircuit <b>B</b> oard
<b>PDF</b>	<b>P</b> robability <b>D</b> ensity <b>F</b> unction
<b>PEEC</b>	<b>P</b> artial <b>E</b> lement <b>E</b> quivalent <b>C</b> ircuit
<b>PJ</b>	<b>P</b> eriodic <b>J</b> itter
<b>PSD</b>	<b>P</b> ower <b>S</b> pectral <b>D</b> ensity
<b>RC</b>	<b>R</b> esistance- <b>C</b> apacitance
<b>RCL</b>	<b>R</b> esistance- <b>C</b> apacitance- <b>I</b> nductance
<b>RJ</b>	<b>R</b> andom <b>J</b> itter
<b>SI</b>	<b>S</b> ignal <b>I</b> ntegrity
<b>SoC</b>	<b>S</b> ystem <b>o</b> n <b>C</b> hip
<b>SPICE</b>	<b>S</b> imulation <b>P</b> rogram with <b>I</b> ntegrated <b>C</b> ircuit <b>E</b> mphasis
<b>STFT</b>	<b>S</b> hort- <b>T</b> ime <b>F</b> ourier <b>T</b> ransform
<b>TD</b>	<b>T</b> ime <b>D</b> omain
<b>TDFE</b>	<b>T</b> ime <b>D</b> omain <b>F</b> inite <b>E</b> lement
<b>TDR</b>	<b>T</b> ime- <b>D</b> omain <b>R</b> eflectometer
<b>TSMC</b>	<b>T</b> aiwan <b>S</b> emiconductor <b>M</b> anufacturing <b>C</b> ompany
<b>VHDL</b>	<b>V</b> ery high-speed integrated circuit <b>H</b> ardware <b>D</b> escription <b>L</b> anguage
<b>WT</b>	<b>W</b> avelet <b>T</b> ransform