Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department

Design of Low Power High Speed Arithmetic Logic Unit (ALU)

A Thesis

Submitted in partial fulfillment for the requirements

of the degree of Master of Science in Electrical Engineering

(Electronics and Communications Engineering)

Submitted By

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Statement

This dissertation is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the department of Electronics and Communications Engineering, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or qualifications at any other university or institution.

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