



Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department

Design of Low Power High Speed Arithmetic Logic Unit (ALU)

A Thesis

Submitted in partial fulfillment for the requirements
of the degree of Master of Science in Electrical Engineering
(Electronics and Communications Engineering)

Submitted By

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Statement

This dissertation is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the department of Electronics and Communications Engineering, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or qualifications at any other university or institution.

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Table of Contents

TABLE OF CONTENTS	i
LIST OF FIGURES	vi
LIST OF TABLES	xi
LIST OF ABBREVIATIONS	xii
ABSTRACT	1
CHAPTER 1: INTRODUCTION	3
1.1 Problem Statement and Contribution.....	3
1.2 Organization	4
CHAPTER 2: HISTORY OF FLOATING POINT UNITS ON FPGAs	6
CHAPTER 3: DIGITAL DESIGN	12
3.1 Application Specific Integrated Circuits (ASICs).....	12
3.2 Programmable Logic Devices (PLDs).....	14
3.2.1 Introduction	14
3.2.2 Simple Programmable Logic Devices (SPLDs).....	15
3.2.3 Complex Programmable Logic Devices (CPLDs).....	18
3.3 Field Programmable Gate Arrays (FPGAs).....	19
3.3.1 Comparing FPGAs to ASICs and CPLDs.....	20
3.3.2 Xilinx FPGAs.....	21
3.3.2.1 Architecture.....	21

3.3.2.2	Interconnects Technology.....	22
3.3.2.3	Virtex FPGA Family.....	23
3.3.2.4	Speed Grades.....	26
3.4	FPGAs Design Flow.....	27
CHAPTER 4: FLOATING POINT ARITHMETIC		31
4.1	Fixed and Floating Point Representation.....	31
4.2	IEEE-754 Standard for Floating Point Representation.....	33
4.2.1	Numerical Encoding.....	33
4.2.2	Normalized and Denormalized Numbers.....	35
4.2.3	Special Values.....	36
4.2.4	Range of Floating Point Numbers.....	36
4.2.5	Exceptions.....	37
4.2.6	Rounding Modes.....	37
4.3	Floating Point Arithmetic.....	39
4.3.1	Floating Point Multiplication Algorithms.....	39
4.3.2	Floating Point Addition/Subtraction Algorithms	43
CHAPTER 5: PROPOSED FLOATING POINT UNIT ARCHITECTURE.....		47
5.1	Design Specifications of Proposed FPU.....	47
5.1.1	Floating Point Representation.....	47
5.1.2	Power Considerations.....	49
5.1.3	Pipelined Architecture.....	50
5.2	Proposed FP Multiplier Unit	51

5.2.1	Introduction.....	51
5.2.2	Zero Detect Module.....	55
5.2.3	Add Exponent Module	57
5.2.4	Multiplier Module.....	58
5.2.4.1	Multiplier (8 by 8) Sub-Module.....	60
5.2.4.2	Partial Fraction Adjust Sub-Module.....	61
5.2.4.3	Add Partial Fractions Sub-Module.....	61
5.2.4.4	Final Result Sub-Module.....	62
5.2.5	Post Normalize Module.....	65
5.2.5.1	Post Normalize Sub-Module.....	66
5.2.5.2	Exception Detection Sub-Module	67
5.2.6	Rounding Module.....	69
5.2.6.1	REN Sub-Module.....	69
5.2.6.2	Overflow Recheck Sub-Module.....	72
5.2.6.3	Output Sub-Module.....	73
5.2.1.7	The FP Multiplier Unit Behavioral Simulation.....	74
5.3	Proposed FP Adder/Subtractor Unit.....	76
5.3.1	Introduction.....	76
5.3.2	Unpack Module.....	79
5.3.3	Swap Module	80
5.3.4	Zero Detect Module.....	82
5.3.5	Pre-Normalize Module.....	84
5.3.6	Add/Subtract Module.....	86

5.3.6.1	Pre-Add/Subtract Sub-Module.....	87
5.3.6.2	Zeros Flag Update Sub-Module.....	89
5.3.6.3	Adder Sub-Module.....	90
5.3.7	Post Normalize Module.....	91
5.3.7.1	Zeros Count Sub-Module.....	92
5.3.7.2	Exponent Adjust Sub-Module.....	93
5.3.7.3	Mantissa Normalize Sub-Module.....	95
5.3.8	Rounding Module.....	96
5.3.8.1	REN Sub-Module.....	96
5.3.8.2	Final Sub-Module.....	98
5.3.9	The FP Adder/Subtractor Behavioral Simulation.....	99
CHAPTER 6:	DESIGN IMPLEMENTATION AND RESULTS.....	101
6.1	Design Optimization.....	101
6.1.1	Optimization Techniques.....	101
6.1.2	FP Adder/Subtractor Optimization.....	103
6.1.3	FP Multiplier Unit Optimization.....	105
6.2	Implementation Results.....	106
6.3	Comparison with Previous Implementations	107
6.3.1	Comparison of FP Adder Unit Implementation Results.....	109
6.3.2	Comparison of FP Multiplier Unit Implementation Results.....	111
6.5	Power Analysis	111
6.5	Post Route Simulations	113
6.5.1	FP Adder/Subtractor Unit Timing Simulation.....	113

6.5.2	FP Multiplier Unit Timing Simulation.....	114
CHAPTER 7: CONCLUSIONS and FUTURE WORK.....		116
7.1	Conclusions.....	116
7.2	Future Work.....	117
REFERENCES.....		118

List of Figures

Figure 3.1	Basic Architecture of PLA.....	16
Figure 3.2	Basic Architecture of PROM.....	16
Figure 3.3	Basic Architecture of PAL.....	17
Figure 3.4	Basic Architecture of GAL.....	17
Figure 3.5	Simple Schematic of a CPLD.....	18
Figure 3.6	Basic Architecture of a Xilinx FPGA.....	21
Figure 3.7	Simplified Xilinx Logic Cell.....	22
Figure 3.8	Simplified Schematic of Virtex-4 Slice.....	25
Figure 3.9	Simplified Schematic of Virtex-5 Slice.....	26
Figure 3.10	Digital Design Flow.....	27
Figure 4.1	IEEE Format of Single Precision FP Number.....	34
Figure 4.2	LOD vs. LOP Algorithms.....	45
Figure 5.1	Simplified Block Diagram of FP Multiplier Unit	51
Figure 5.2(a)	Detailed Block Diagram of FP Multiplier Unit.....	53
Figure 5.2(b)	Detailed Block Diagram of FP Multiplier Unit.....	54
Figure 5.3	Symbol of Unpack Module in the FP Multiplier Unit.....	56
Figure 5.4	Behavioral Simulation of the Unpack Module in the FP Multiplier Unit.....	56
Figure 5.5	Symbol of the Add Exponent Module in the FP Multiplier Unit.....	58
Figure 5.6	Behavioral Simulation of the Add Exponent Module in the FP Multiplier Unit.....	58

Figure 5.7	The Three Parallel Multiplications Performed in the Block Multiplication Algorithm.....	59
Figure 5.8	Details of Mantissa A * B0 Multiplication.....	59
Figure 5.9	Block Diagram of the Block Multiplier.....	60
Figure 5.10	Shift Operations Performed to Align the Partial Fractions for Addition...	61
Figure 5.11	Dividing the Partial Fraction to prepare them for Addition.....	62
Figure 5.12	Block Diagram of Multiplier Module in the FP Multiplier Unit.....	63
Figure 5.13	Behavioral Simulation of the Multiplier (8 by8) Sub-Module.....	64
Figure 5.14	Behavioral Simulation of the Partial Fraction Adjust Sub-Module.....	64
Figure 5.15	Behavioral Simulation of the Add Partial Fractions Sub-Module.....	65
Figure 5.16	Behavioral Simulation of the Final Result Sub-Module.....	65
Figure 5.17	Symbol of the Post Normalize Sub-Module in the FP Multiplier Unit....	67
Figure 5.18	Behavioral Simulation of the Post Normalize Sub-Module in the FP Multiplier Unit.....	67
Figure 5.19	Symbol of the Exception Detection Sub-Module in the FP Multiplier Unit.....	68
Figure 5.20	Behavioral Simulation of the Exception Detection Sub-Module in the FP Multiplier Unit.....	68
Figure 5.21	Symbol of the REN Sub-Module in the FP Multiplier Unit.....	70
Figure 5.22	Behavioral Simulation of the REN Sub-Module in the FP Multiplier Unit when the Resultant Mantissa to be rounded is Even.....	70
Figure 5.23	Behavioral Simulation of the REN Sub-Module in the FP Multiplier Unit when the Resultant Mantissa to be rounded is Odd.....	71

Figure 5.24	Symbol of the Overflow Recheck Sub-Module in the FP Multiplier.....	72
Figure 5.25	Behavioral Simulation of the Overflow Recheck Sub-Module in the FP Multiplier Unit.....	73
Figure 5.26	Symbol of the Final Module in the FP Multiplier Unit.....	73
Figure 5.27	Behavioral Simulation of the Final Module in the FP Multiplier Unit....	74
Figure 5.28	Symbol of the FP Multiplier Unit.....	74
Figure 5.29	Behavioral Simulation of the FP Multiplier Unit.....	75
Figure 5.30	Simplified Block Diagram of FP Adder/Subtractor Unit.....	76
Figure 5.31a	Detailed Block Diagram of FP Adder/Subtractor Unit.....	78
Figure 5.31b	Detailed Block Diagram of FP Adder/Subtractor Unit.....	78
Figure 5.32	Symbol of the Unpack Module in the FP.....	80
Figure 5.33	Behavioral Simulation of the Unpack Module in the FP Adder/Subtractor Unit.....	80
Figure 5.34	Symbol of the Swap Module in the FP Adder/Subtractor Unit.....	81
Figure 5.35	Behavioral Simulation of the Swap Module in the FP Adder/Subtractor Unit.....	82
Figure 5.36	Symbol of the Zero Detect Module in the FP Adder/Subtractor Unit.....	83
Figure 5.37	Behavioral Simulation of the Zero Detect Module in the FP Adder/Subtractor Unit.....	84
Figure 5.38	Format of 28 bit Mantissa.....	84
Figure 5.39	Symbol of the Pre-normalize Module in the FP Adder/Subtractor Unit...	86
Figure 5.40	Behavioral Simulation of the Pre-normalize Module in the FP Adder/Subtractor Unit.....	86

Figure 5.41	Symbol of the Pre-Add/Subtract Sub-Module in the FP Adder/Subtractor Unit.....	87
Figure 5.42	Behavioral Simulation of the Pre-Add/Subtract Sub-Module in the FP Adder/Subtractor Unit for Mantissa B greater than Mantissa A.....	88
Figure 5.43	Behavioral Simulation of the Pre-Add/Subtract Sub-Module in the FP Adder/Subtractor Unit for Mantissa A greater than Mantissa B.....	88
Figure 5.44	Symbol of the Zero-Update Sub-Module in the FP Adder/Subtractor Unit.....	89
Figure 5.45	Behavioral Simulation of the Zero Update Sub-Module in the FP Adder/Subtractor Unit.....	89
Figure 5.46	Symbol of the Adder Sub-Module in the FP Adder/Subtractor Unit.....	90
Figure 5.47	Behavioral Simulation of the Adder Sub-Module in the FP Adder/Subtractor Unit.....	91
Figure 5.48	Symbol of Zeros Count Sub-Module in the FP Adder/Subtractor Unit....	92
Figure 5.49	Behavioral Simulation of Zeros Count Sub-Module in the FP Adder/Subtractor Unit.....	93
Figure 5.50	Symbol of the Exponent Adjust Sub-Module in the FP Adder/Subtractor Unit.....	94
Figure 5.51	Behavioral Simulation of the Exponent Adjust Sub-Module in the FP Adder/Subtractor Unit.....	94
Figure 5.52	Symbol of Mantissa Normalize Sub-Module in the FP Adder/Subtractor Unit.....	95
Figure 5.53	Behavioral Simulation of Mantissa Normalize Sub-Module in the	

	FP Adder/Subtractor Unit.....	96
Figure 5.54	Symbol of the REN Sub-Module in the FP Adder/Subtractor Unit.....	97
Figure 5.55	Behavioral Simulation of REN Sub-Module in the FP Adder/Subtractor Unit.....	97
Figure 5.56	Symbol of the Final Sub-Module in the FP Adder/Subtractor Unit.....	98
Figure 5.57	Behavioral Simulation of Final Sub-Module in the FP Adder/Subtractor Unit.....	98
Figure 5.58	Symbol of the FP Adder/Subtractor Unit.....	99
Figure 5.59	Behavioral Simulation of the FP Adder/Subtractor Unit.....	99
Figure 6.1	Offset in Time Constraint.....	103
Figure 6.2	FP Adder/Subtractor Unit Power Consumption vs. Frequency.....	112
Figure 6.3	FP Multiplier Unit Power Consumption vs. Frequency.....	113
Figure 6.4	Input Test Bench of the FP Adder/Subtractor at 3.2ns.....	114
Figure 6.5	Output of the FP Adder/Subtractor Test Bench.....	114
Figure 6.6	Input Testbench for FP Multiplier at 2.5ns	115
Figure 6.7	Output of the FP Multiplier Test Bench	115