AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications Engineering Department

Modeling of Analog Building Blocks by Using Standard Hardware Description Language

A Thesis
Submitted in partial fulfillment of the requirements of the degree of
Master of Science in Electrical Engineering

Submitted by
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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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The very high Speed Integrated circuit Hardware Description Language (VHDL) has been primarily used to define and simulate digital integrated circuits. However, most integrated circuits contain both analog and digital circuits. Conventionally, analog and digital circuits are described by different languages and simulated separately. It is desirable to describe mixed analog-digital circuits by the same language and simulate them on the same simulator so that the entire design characteristics are verified through simulation.

This thesis presents modeling of analog blocks by a language used for describing digital hardware. This modeling approach, allows simulating analog circuits by adopting an event driven standard simulator (such as VHDL's simulator) .VHDL language has been used to define and simulate digital integrated circuits. Modeling by VHDL allows analog digital interface simulations. Also, it allows the designers to reconfigure the design by themselves. Transistor level simulators need much time to verify the circuit performance. VHDL is technology independent so it avoids large simulation time, so this modeling approach allows fast simulations. Modeling by VHDL allows low development cost and short time to the market

This thesis begins with the description of how to model analog circuit by using VHDL followed by modeling of open loop operational amplifier (Op-amp). Also Op-amp applications where modeled Then some compensation technique were applied to these circuits. The results before and after compensation were shown. SPICE simulation results confirm the VHDL simulation results are also given. Then the topic of analog filters comes into discussion. Important analog filters are presented (KHN and Tow Thomas).The ideal filter is modeled. Then it’s remodeled by taking Op-amp second order effects. Also compensation applied to these filters. Ideal and compensated responses compared together. Then the current feedback operational amplifier (CFOA) is shown. CFOA is compared with the voltage operational amplifier (VOA). Finally CFOA applications are shown.

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