Ain Shams University
Faculty of Engineering
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Data Converters For High Speed Serial Links

A thesis
submitted in partial fulfillment of the requirements of the degree of Master of Science in Electrical Engineering

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AIN SHAMS UNIVERSITY
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Electronics Engineering and Electrical Communications

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by

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

Khaled Mohamed Ashraf Mohamed Alaa El-Din El-Gammal "Data Converters For High Speed Serial Links", Master of Science dissertation, Ain Shams University, 2016.
This thesis presents a high speed ADC, to be used as an analog-front-end in an digital receiver chain, in serial link applications. The use of digital equalizers in the receiver chain provide higher programmability. Thus, it can equalize high-attenuation channels.

Digital Equalizers can be easily scaled with different technology nodes. Thus, using digital equalizers is preferred in serial link receivers. This increases the interest in high-speed, low-power ADCs to be used in the receiver front-end.

The high-speed ADC, discussed in this thesis, eliminated the need for any digital calibration. This is done while acheivieng a competitive FOM, when compared to state-of-art ADCs.

Two design appproaches are shown in this thesis, each is clearly discussed with its advantages and drawbacks. A full-system analysis, is also shown, in terms of noise budgeting for each subblock, along with speed and linearity requirements.

The first design approach, utilized the usage of a modified clocking scheme, to simplify the design of main ADC subblocks such as: boot-strapped sample-and-hold, and preamplifiers, and comparator latch. This acheived a superior FOM of 115 fJ/conversion-step, and a power consumption of 13 mW from 1.2V supply. This design had some drawbacks, which will be further discussed. These drawbacks are solved in the second design approach.

The second design approach, used the conventional clocking with a modified boot-strapped sample-and-hold, and comparator preamplifiers. This enabled to solve the drawbacks of the first design, acheiving an INL and DNL of less than $0.5LSB$, and a FOM of 182 fJ/conversion-steps. This design consumes 23 mW from 1.2V supply. A comparison is made between the ADC performance metrics of this ADC, and the state-of-art ADCs stated in the survey.

Key words: Analog-to-digital conversion, clocking scheme, time-interleaved ADC, flash ADC, comparators, clock delay, sample-and-hold.