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FACULTY OF ENGINEERING

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Development of Channel Coder for WCDMA Mobile Phone

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

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Over the last few years, great advances have been made in mobile communication technology. The third generation (3G) mobile systems provide further improved network capacity, high speed packet data and voice and real-time multimedia services. WCDMA has become the major 3G air interface in the world. Modern wireless communication systems utilize certain digital signaling techniques known as channel coding to improve performance, efficiency and to achieve reliable communication over noisy and fading channels.

WCDMA employs convolutional coding to encode voice and MPEG4 applications at maximum data rate 2 Mbps. Viterbi algorithm is the powerful method for decoding convolutional codes. Several hardware architectures are used to implement Viterbi decoder. Serial or parallel schemes are used to implement ACS computation block. Also two main hardware architectures are used to implement Survivor memory unit of Viterbi decoder, Trace back (TB) method and Register Exchange (RE) method. The complexity of Viterbi decoding is an exponential function of the constraint length. WCDMA requires decoder with constraint length of 9 (256 states), which poses an implementation challenge.

In this thesis, Matlab simulation Model as well as hardware architecture of WCDMA Viterbi decoder was designed with specifications according to 3GPP standard, where the code rates are 1/2 and 1/3. The proposed decoder uses serial architecture combined with modified version of register exchange method for achieving small area. The hardware prototype is successfully implemented on Xilinx Virtex-5 family. The core occupies about 5% of total FPGA slices & 1% of block RAM resources. Furthermore, the achievable core throughput is 5 Mbps, which exceeds target speed. Also BER performance shows that at $E_b/N_0 = 10^{-3}$, the coding gain of approximately 4.8 dB is achieved for code rate = 1/2 and 5.1 dB for code rate = 1/3.

Summary

This dissertation focuses on the convolutional coding as one of channel coding schemes adopted in 3G-WCDMA Mobile systems. It demonstrates the design and implementation of channel Viterbi decoder on FPGA. The dissertation is divided into six chapters, in addition to table of contents, list of figures, tables and references.

Chapter one: It includes a brief history for the Mobile telecommunication three generations, and shows the concept of channel coding. Then an overview on WCDMA transceiver system is presented. This chapter finishes with thesis outline.

Chapter two: This chapter describes the encoder structure for convolutional codes. Also, the main decoding strategy, based on the Viterbi Algorithm, is illustrated. Finally, the hard-decision and soft decision Viterbi decoding types is presented.

Chapter three: This chapter discusses the main parts of the Viterbi decoder for practical hardware implementation. Different hardware architectures and topologies of the main blocks, Branch metric unit (BMU) & Add-Compare-Select unit (ACSU) & Surviving Memory unit (SMU), are demonstrated. Then, a survey on previous work of Viterbi decoder design for wireless applications is stated.

Chapter four: This chapter provides a brief overview on the architecture of Field Programmable Gate Arrays and specially the main features of Xilinx Virtex-5 FPGA. Finally, the digital design flow for Xilinx FPGA is explained.

Chapter Five: This chapter illustrates in detail the proposed architecture and implementation steps of WCDMA Viterbi decoder with the specifications that comply with 3GPP standard, where the code rates are 1/2 and 1/3. The proposed decoder uses serial architecture combined with modified version of register exchange method for achieving small area. The Viterbi decoder was implemented both in Software and Hardware. The Software implementation has been carried out using Matlab simulation tool. Then Hardware implementation was performed using VHDL, synthesis and simulations were carried out using Xilinx ISE and Modelsim tools targeting Virtex-5 FPGA device. Finally, the results of simulations, FPGA resource utilization, operating frequency, throughput decoding rate, BER performance evaluation and comparison the results with previous work are presented.**Chapter Six:** This chapter consists of the conclusions and states the future work in this topic.

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List of Abbreviations

ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
ACSU	Add Compare Select Unit
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
BMU	Branch Metric Unit
CRC	Cyclic Redundancy Check
DSP	Digital Signal Processor
DAC	Digital to Analog Converter
DB	Decision Bit
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
GSM	Global System for Mobile Communication
OVFS	Orthogonal Variable Factor Spreading
PM	Path Metric
PE	Processing Element
RE	Register-Exchange
SNR	Signal to Noise Ratio
SMU	Survivor Memory Unit
TB	Trace Back
UMTS	Universal Mobile Telecommunication System
VD	Viterbi Decoder
VLSI	Very Large Scale Integrated circuits
VHDL	VLSI Hardware Description Language
WCDMA	Wideband Code Division Multiple Access
1G	First Generation
2G	Second Generation
3G	Third Generation
3GPP	Third Generation Partnership Project