Ain Shams University
Faculty of Engineering
Electronics and Communications Department

Power Estimation Using Emulation

A thesis
submitted in partial fulfillment of the requirements of the degree of
Master of Science in Electrical Engineering

Submitted by

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Power Estimation Using Emulation

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Masters of Science Dissertation
Electronics and communications Department
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Abstract

System level power estimation became an essential aspect in order to address today's increasing electronic design challenges such as high performance and low power consumption at minimum costs. Contemporary advanced software applications such as multimedia, radio, GPS and other mobile applications impose a strict power consumption scheme. Therefore, in order to meet real-time performance constraints at high quality of services, functional, timing and power architectural behavior of underlying hardware should be analyzed. Virtual Platforms (VPs) are leading the Electronic System Level (ESL) design methodology mutation for architecture exploration, performance analysis and early software development. Virtual platforms can emulate actual hardware behavior at very early design stages using high-abstraction software models. They are increasingly adopted in industry to simulate today's complex Multi-Processor System-on-Chip (MPSoC) designs. Moreover, they can be used by software engineers to analyze their software effect on hardware design power consumption. In this thesis, a fast, yet accurate, multi-core virtual platform is developed and validated through which system-level power consumption can be estimated. The developed VP is modeled in accordance with Transaction Level Modeling (TLM) methodology.

Furthermore, the proposed TLM VP supports an Instruction Set Simulator (ISS) that efficiently utilizes underlying multi-core host processor to run multi-thread applications at high speed. The ISS model is based on Dynamic binary Translation (DBT) technology. A unique SystemC synchronization approach among emulated target cores is adopted. In addition, instruction-based computational power estimation methodology is demonstrated. Overall peripherals power estimation techniques based on computation, communication, state, clock tree and static power evaluation are also introduced.

Using EEMBC CoreMark, Dhrystone and Whetstone benchmarks, an average percentage error of 10% in power consumption estimation at TLM level is obtained versus corresponding measured real HW board power consumption. Using SPLASH-2 and EEMBC CoreMark benchmarks, the presented TLM VP, emulating the NXP Sabre-Lite IMX6Q Quad-Core Cortex-A9 board, achieves on average 3.9X performance speedup over corresponding baseline QEMU machine that is equivalent to 15% of the real HW board speed.

Key words: Power Estimation, Virtual Platform, Multi-core, TLM, ISS, Power evaluation, MPSoC.

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