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Digital Techniques in Frequency Synthesis
A Thesis

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Abstract

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The thesis contains a study for some Digital Techniques in Frequency Synthesis that makes the use of an All Digital PLL possible. At the heart of the All Digital PLL lies a Digitally Controlled Oscillator which deliberately avoids any analog tuning voltage controls. We address two of the main issues of the Digitally Controlled Oscillator; that is its center frequency (f_{DCO}) variations & tuning gain (K_{DCO}) variations.

To mitigate the center frequency variations, we propose a new fast automatic tuning algorithm for LC based oscillators. The proposed algorithm is verified over a wide range of initial Digitally Controlled Oscillator frequencies & phases to guarantee robust operation over all process corner variations with the worst case tuning time being only 7.2μsec.

To mitigate tuning gain variations, we study a fast tuning gain estimation & calibration algorithm. This tuning gain calibration makes it possible to use a two point modulation scheme to transmit Frequency Shift Keying data at symbol rates much higher than the loop bandwidth upto the Nyquist frequency of half the reference frequency.

We use a Verilog model to verify the successful All Digital PLL functionality & performance transitioning from reset to center frequency automatic tuning to tuning

gain estimation & calibration to Frequency Shift Keying data transmission. Also when used as a local oscillator, the implemented All Digital PLL has spurious tones at only -98dBc.

Key words: All Digital PLL, Digitally Controlled Oscillator, Automatic Tuning, Tuning Gain Estimation, Tuning Gain Calibration, Two Point Modulation, Frequency Shift Keying.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In this chapter we present the motivation behind this work, briefly introduce the different frequency synthesis techniques & finally we present the thesis outline.

1.1. Motivation

With the explosive growth of the wireless communication industry, research related to communication circuits and architectures has received a great deal of attention. The major issues being addressed are low-cost, low-voltage, and low-power designs, which combine necessary performance with the ability to be manufactured economically in high volumes.

The use of deep-submicrometer CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits. Consequently, a new research focuses on finding digital architectural solutions to these integration problems. Modern transceivers are expected to operate over a

wide range of frequencies. Although crystal oscillators offer high spectral purity, they cannot be tuned over a wide range of frequencies. Hence, some form of frequency synthesis is employed by these transceivers.

1.2. Frequency Synthesis

The term frequency synthesizer generally refers to an active electronic device Figure 1-1 that accepts some frequency reference (FREF) input signal of a very stable frequency f_R and then generates frequency output as commanded by the frequency command word (FCW), whereby the stability, accuracy, and spectral purity of the output correlate with the performance of the input reference. The desired value of the output frequency is an FCW multiple (generally, a real number) of the reference frequency according to the equation

$$f_{out} = FCW \cdot f_{ref} \tag{1.1}$$

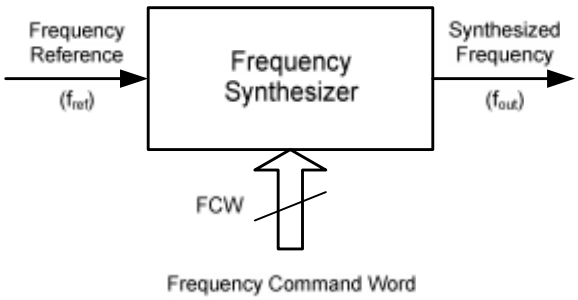

Figure 1-1 Frequency Synthesis

Interestingly, the definition above does not specify the shape of the synthesized output. It could be a sinusoid or a rectangular signal (Figure 1-2). The frequency and phase information is preserved in either a continuous-time waveform fit to the ideal sinusoid or in edge transition times, respectively. A clear advantage of the rectangular digital signal is that it is more useful for digital CMOS process technology.

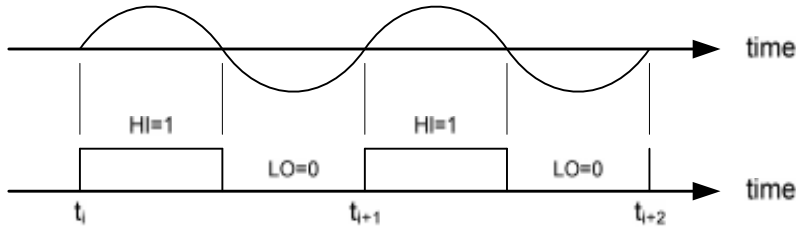

Figure 1-2 Possible outputs of a synthesizer: sinusoidal and digital waveforms

1.3. Frequency Synthesis Techniques

There are three major conventional frequency synthesis techniques:

- Direct analog mix/filter/divide
- Direct digital
- Indirect or phase-locked loop
- Hybrids: any combination of the three methods above

Each of these methods has its own advantages and disadvantages; hence, each application requires selection based on the most acceptable combination of compromises.

1.3.1. Direct Analog Synthesis

Direct analog synthesis, also called mix/filter/divide, uses frequency multipliers, dividers, and other mathematical manipulations to produce the desired new frequency [Reinhardt 86]. The process is called direct because the error correction process is avoided; hence, the quality of the output correlates directly with the quality of the input. Phase noise is typically excellent because the direct process and switching speed can be very fast. Unfortunately, a broadband mix/filter/divide synthesizer requires many references, which makes it extremely expensive. Because of its high cost and high power disadvantages, the direct analog synthesis method is used primarily in instrumentation and is not practical for low-power portable applications such as mobile communication terminals.

1.3.2. Direct Digital Synthesis

Direct digital frequency synthesis (DDFS) is the most recently developed frequency synthesis technique, dating from the early 1970s [Tierney 71]. A DDFS system uses logic and memory to construct the desired output signal digitally, and a data conversion device [a digital-to-analog converter (DAC)] to convert it from the digital to the analog domain, as shown in Figure 1-3. Therefore, the DDFS method of constructing a signal is almost entirely digital, and the precise amplitude, frequency, and phase are known and controlled at all times. For these reasons, the switching speed is extremely high, but the power consumption could be excessive at high clock frequencies. The DDFS method is not entirely digital in the true sense of the word since it requires a DAC and a low-pass filter (LPF) to attenuate spurious frequencies produced by the digital switching. In addition, a very stable frequency reference clock of at least three times the output frequency is required. Considering this and the fact that the DAC and LPF might be difficult to build and would consume excessive amount of power at gigahertz operational frequency, the DDFS solution is not acceptable for radio-frequency (RF) applications such as mobile communication terminals.

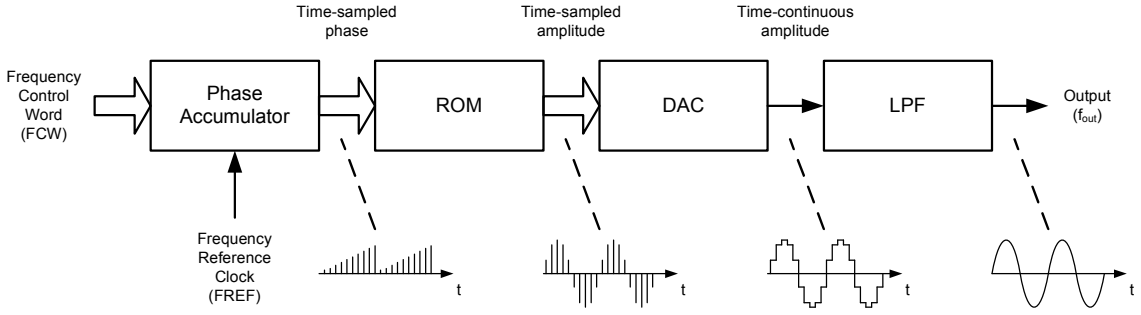

Figure 1-3 Direct digital frequency synthesis [Tierney 71].

Due to its digital waveform reconstruction nature, the DDFS technique is best suited for implementing wideband transmit modulation as well as fast channel hopping schemes [Tan 95]. As an example, Figure 1-4 shows the phase accumulator front end of a DDFS system