



Ain Shams University  
Faculty of Engineering  
Electronics and Communications Department

# Digital Techniques in Frequency Synthesis

## A Thesis

Submitted in partial fulfillment for the requirements of Master of Science  
degree in Electrical Engineering

Submitted by:

**Mohammed Ibrahim Ibrahim El-Shennawy**

B.Sc. of Electrical Engineering  
(Electronics and Communications Department)  
Ain Shams University, 2004.

Supervised by:

Dr. Safwat Mahrous Mahmoud  
Dr. Emad El-Din Mahmoud Hegazi  
Dr. Hani Fikry Ragai

Cairo 2011



جامعة عين شمس  
كلية الهندسة  
قسم الالكترونيات و الاتصالات

## الاساليب الرقمية لتركيب الترددات

رسالة بحث للحصول على

درجة الماجستير فى الهندسة الكهربائية  
الالكترونيات و الاتصالات

مقدمة من:

م/محمد ابراهيم ابراهيم الشناوى

بكالوريوس فى الهندسة الكهربائية

(الالكترونيات و الاتصالات)

جامعة عين شمس , ٢٠٠٤

تحت إشراف:

أ.د./ صفوت محروس محمود

أ.د./ عماد الدين محمود حجازى

أ.د./ هانى فكرى رجائى

القاهرة ٢٠١١

# Abstract

Mohammed Ibrahim Ibrahim El-Shennawy, Digital Techniques in Frequency Synthesis

Faculty of Engineering, Ain Shams University, 2011

The thesis contains a study for some Digital Techniques in Frequency Synthesis that makes the use of an All Digital PLL possible. At the heart of the All Digital PLL lies a Digitally Controlled Oscillator which deliberately avoids any analog tuning voltage controls. We address two of the main issues of the Digitally Controlled Oscillator; that is its center frequency ( $f_{DCO}$ ) variations & tuning gain ( $K_{DCO}$ ) variations.

To mitigate the center frequency variations, we propose a new fast automatic tuning algorithm for LC based oscillators. The proposed algorithm is verified over a wide range of initial Digitally Controlled Oscillator frequencies & phases to guarantee robust operation over all process corner variations with the worst case tuning time being only 7.2 $\mu$ sec.

To mitigate tuning gain variations, we study a fast tuning gain estimation & calibration algorithm. This tuning gain calibration makes it possible to use a two point modulation scheme to transmit Frequency Shift Keying data at symbol rates much higher than the loop bandwidth upto the Nyquist frequency of half the reference frequency.

We use a Verilog model to verify the successful All Digital PLL functionality & performance transitioning from reset to center frequency automatic tuning to tuning

gain estimation & calibration to Frequency Shift Keying data transmission. Also when used as a local oscillator, the implemented All Digital PLL has spurious tones at only -98dBc.

Key words: All Digital PLL, Digitally Controlled Oscillator, Automatic Tuning, Tuning Gain Estimation, Tuning Gain Calibration, Two Point Modulation, Frequency Shift Keying.

# Contents

Chapter 1 .....	1
Introduction.....	1
1.1. Motivation.....	1
1.2. Frequency Synthesis .....	2
1.3. Frequency Synthesis Techniques.....	3
1.3.1. Direct Analog Synthesis .....	3
1.3.2. Direct Digital Synthesis .....	4
1.3.3. Indirect Synthesis Using Phase Locking.....	6
1.3.4. Hybrid Structure Frequency Synthesis .....	7
1.4. Frequency Synthesizers for Mobile Communications .....	8
1.4.1. Integer-N PLL Architecture.....	10
1.4.2. Fractional-N PLL Architecture .....	10
1.4.3. Toward an All-Digital PLL Approach.....	17
1.5. Thesis Outline .....	18
Chapter 2.....	19
ADPLL Basics .....	19
2.1. Introduction.....	19
2.2. ADPLL System.....	21
2.3. Phase Domain Operation .....	22
2.4. Reference Clock Retiming.....	24
2.5. Phase Detection.....	26
2.6. Modulo Arithmetic of Phase Domain Signals .....	27

2.7. Discrete Time Z-Domain Model.....	29
2.8. Linear S-Domain Approximation .....	31
2.9. Summary .....	32
Chapter 3 .....	33
ADPLL Modeling .....	33
3.1. Introduction.....	33
3.2. ADPLL Building Blocks.....	34
3.3. Synchronous Counter with Reset Model .....	35
3.4. Sampler Model.....	36
3.5. Synchronizer Model.....	37
3.6. Phase Detector Model .....	38
3.7. DCO Model.....	39
3.8. ADPLL Top Level Model.....	40
3.9. ADPLL Top Level Test Bench .....	41
3.10. TDC Model .....	43
3.11. Summary .....	45
Chapter 4 .....	46
DCO Automatic Tuning.....	46
4.1. Introduction.....	46
4.2. Existing Automatic Tuning Algorithms.....	47
4.3. Proposed Automatic Tuning Algorithm.....	49
4.4. Fully Custom Block: .....	50
4.4.1. External High Speed Divider by 4: .....	50
4.5. Fully Digital Block: .....	50
4.5.1. Multiplexer:.....	50
4.5.2. Clock Gating: .....	50
4.5.3. Synchronizer: .....	51
4.5.4. Divider by 4: .....	51
4.5.5. Synchronous Counter with Reset:.....	52
4.5.6. Bus Synchronizer:.....	52
4.5.7. Comparator: .....	52
4.6. Algorithm Execution Sequence .....	54

4.7. Algorithm Verilog Code .....	55
4.8. Simulation Results .....	69
4.9. Summary .....	71
Chapter 5 .....	72
$K_{DCO}$ Calibration within the ADPLL .....	72
5.1. Introduction.....	72
5.2. DCO Transfer Function & Gain .....	75
5.3. DCO Gain Normalization .....	75
5.4. Predictive/Closed PLL Operation.....	76
5.5. DCO Gain Estimation using the ADPLL.....	78
5.6. Effect of Incorrect $K_{DCO}$ Estimation .....	81
5.7. Algorithm Verilog Code .....	85
5.8. Simulation Results .....	90
Chapter 6.....	92
The ADPLL as an FSK Transmitter .....	92
6.1. Introduction.....	92
6.2. Test Bench Verilog Code.....	93
6.3. Simulation Results .....	97
6.4. Spurious Tones.....	106
Conclusion .....	110
Future Work .....	112
References.....	113

# List of Figures

Figure 1-1 Frequency Synthesis.....	2
Figure 1-2 Possible outputs of a synthesizer: sinusoidal and digital waveforms .....	3
Figure 1-3 Direct digital frequency synthesis.....	4
Figure 1-4 Phase accumulator front end of a DDS system with frequency modulation .....	5
Figure 1-5 Phase Locked Loop.....	6
Figure 1-6 DDS-PLL hybrid.....	7
Figure 1-7 Typical charge-pump-based PLL for RF wireless applications.....	9
Figure 1-8 Alternating divide ratio of fractional-N PLL .....	11
Figure 1-9 Periodic and deterministic phase error in a fractional-N PLL .....	12
Figure 1-10 Fractional-N PLL incorporating phase interpolation .....	12
Figure 1-11 Fractional-N synthesizer using a $\Sigma\Delta$ -modulated clock divider.....	13
Figure 1-12 MASH-3 $\Sigma\Delta$ digital modulator divider .....	14
Figure 1-13 $\Sigma\Delta$ -divided clock: clock output spectrum (left), phase spectrum (right) .....	15
Figure 1-14 Modulating a wideband fractional-N synthesizer .....	16
Figure 1-15 ADPLL-based RF frequency synthesizer.....	17
Figure 2-1 ADPLL-based RF frequency synthesizer.....	21
Figure 2-2 Concept of synchronizing the clock domains by retiming the FREF. ....	23
Figure 2-3 Hardware implementation of the variable phase & the reference phase .....	25
Figure 2-4 Fractional-N division ratio timing example with $N = 2+(1/4)$ .....	25
Figure 2-5 Modulo arithmetic of the reference and variable phase registers .....	28
Figure 2-6 Rotating vector interpretation of the reference and variable phases. ....	28
Figure 2-7 z-domain model of the type-II ADPLL.....	29



Figure 2-8 Linear s-domain model of the type-II ADPLL. ....	31
Figure 3-1 ADPLL main building blocks .....	34
Figure 3-2 Synchronous counter with reset model .....	35
Figure 3-3 Sampler model .....	36
Figure 3-4 Synchronizer model .....	37
Figure 3-5 Phase detector model.....	38
Figure 3-6 DCO model .....	39
Figure 3-7 ADPLL top level model. ....	40
Figure 3-8 ADPLL top level test bench. ....	41
Figure 3-9 ADPLL top level simulation results.....	42
Figure 3-10 TDC functionality example with FCW = 2+(1/4) .....	44
Figure 3-11 TDC Model .....	44
Figure 3-12 TDC model waveforms. ....	45
Figure 4-1 DCO Auto Tuning simplified block diagram.....	47
Figure 4-2 Proposed DCO Auto Tuning block diagram .....	51
Figure 4-3 Proposed DCO Auto Tuning control signals timing diagram .....	55
Figure 4-4 Simulated Final DCO Frequency vs. Regression Iteration .....	70
Figure 4-5 Simulated Tuning Curve Number vs. Regression Iteration .....	71
Figure 4-6 Simulated Tuning Time vs. Regression Iteration.....	71
Figure 5-1 Normalized DCO block diagram .....	76
Figure 5-2 Two point modulated ADPLL model .....	77
Figure 5-3 DCO gain estimate by measuring tuning word change in response to a fixed frequency jump. ....	79
Figure 5-4 DCO gain estimation flowchart. ....	80
Figure 5-5 Complex plane location of the H(z) zero and pole movement with different values of the DCO gain estimate accuracy $r$ . ....	82
Figure 5-6 Direct modulation transfer function H(f) where $f \approx (f_R/2\pi)(z-1)$ for $f \ll f_R$ , with different values of the DCO gain estimate accuracy $r$ according to [Staszewski 06]......	84
Figure 5-7 Actual direct modulation transfer function H(f) where $f \approx (f_R/2\pi)(z-1)$ for $f \ll f_R$ , with different values of the DCO gain estimate accuracy $r$ according to this work. ....	85
Figure 5-8 $K_{DCO}$ Calibration Simulation Result .....	91
Figure 6-1 ADPLL-based RF frequency synthesizer when used as an FSK transmitter.....	93

Figure 6-2 ADPLL output in the various modes of operation .....	97
Figure 6-3 Zoom in on the DCO Autotuning period .....	98
Figure 6-4 Zoom in on the $K_{DCO}$ estimation period.....	99
Figure 6-5 2.4GHz Center frequency at the start of $K_{DCO}$ estimation .....	100
Figure 6-6 1MHz positive frequency shift.....	101
Figure 6-7 1MHz negative frequency shift.....	102
Figure 6-8 2Mbps data transmission.....	103
Figure 6-9 Zoom in on the FSK data transmission .....	104
Figure 6-10 FSK transmission at $f_R/2$ .....	105
Figure 6-11 Zoom in on the modulating part of the NTW .....	107
Figure 6-12 FFT of the modulating part of the NTW .....	108
Figure 6-13 ADPLL measured output spectrum from [Staszewski 03a] .....	109

# List of Tables

Table 3-1 ADPLL simple frequency plan.....	42
Table 4-1 Regression Test Bench Results Summary .....	70
Table 6-1 Measured key synthesizer performance from [Staszewski 03a] .....	109

# Chapter 1

## Introduction

In this chapter we present the motivation behind this work, briefly introduce the different frequency synthesis techniques & finally we present the thesis outline.

### 1.1. Motivation

With the explosive growth of the wireless communication industry, research related to communication circuits and architectures has received a great deal of attention. The major issues being addressed are low-cost, low-voltage, and low-power designs, which combine necessary performance with the ability to be manufactured economically in high volumes.

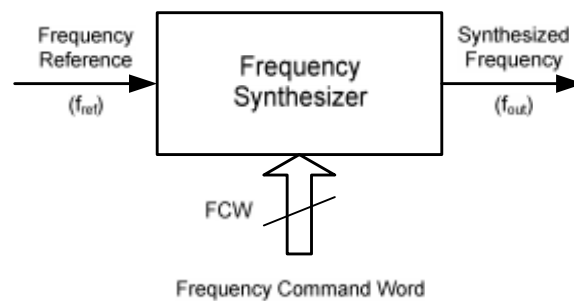
The use of deep-submicrometer CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits. Consequently, a new research focuses on finding digital architectural solutions to these integration problems. Modern transceivers are expected to operate over a

wide range of frequencies. Although crystal oscillators offer high spectral purity, they cannot be tuned over a wide range of frequencies. Hence, some form of frequency synthesis is employed by these transceivers.

## 1.2. Frequency Synthesis

The term frequency synthesizer generally refers to an active electronic device Figure 1-1 that accepts some frequency reference (FREF) input signal of a very stable frequency  $f_R$  and then generates frequency output as commanded by the frequency command word (FCW), whereby the stability, accuracy, and spectral purity of the output correlate with the performance of the input reference. The desired value of the output frequency is an FCW multiple (generally, a real number) of the reference frequency according to the equation

$$f_{out} = FCW \cdot f_{ref} \quad (1.1)$$



**Figure 1-1 Frequency Synthesis**

Interestingly, the definition above does not specify the shape of the synthesized output. It could be a sinusoid or a rectangular signal (Figure 1-2). The frequency and phase information is preserved in either a continuous-time waveform fit to the ideal sinusoid or in edge transition times, respectively. A clear advantage of the rectangular digital signal is that it is more useful for digital CMOS process technology.

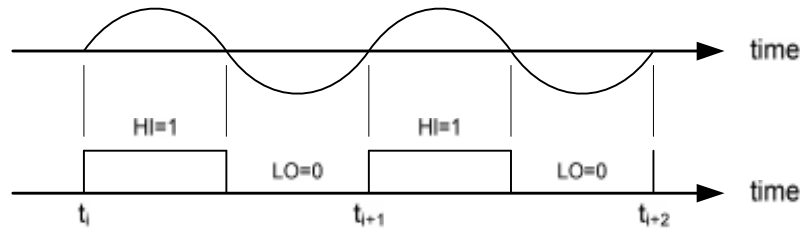


Figure 1-2 Possible outputs of a synthesizer: sinusoidal and digital waveforms

## 1.3. Frequency Synthesis Techniques

There are three major conventional frequency synthesis techniques:

- Direct analog mix/filter/divide
- Direct digital
- Indirect or phase-locked loop
- Hybrids: any combination of the three methods above

Each of these methods has its own advantages and disadvantages; hence, each application requires selection based on the most acceptable combination of compromises.

### 1.3.1. Direct Analog Synthesis

Direct analog synthesis, also called mix/filter/divide, uses frequency multipliers, dividers, and other mathematical manipulations to produce the desired new frequency [Reinhardt 86]. The process is called direct because the error correction process is avoided; hence, the quality of the output correlates directly with the quality of the input. Phase noise is typically excellent because the direct process and switching speed can be very fast. Unfortunately, a broadband mix/filter/divide synthesizer requires many references, which makes it extremely expensive. Because of its high cost and high power disadvantages, the direct analog synthesis method is used primarily in instrumentation and is not practical for low-power portable applications such as mobile communication terminals.

### 1.3.2. Direct Digital Synthesis

Direct digital frequency synthesis (DDFS) is the most recently developed frequency synthesis technique, dating from the early 1970s [Tierney 71]. A DDFS system uses logic and memory to construct the desired output signal digitally, and a data conversion device [a digital-to-analog converter (DAC)] to convert it from the digital to the analog domain, as shown in Figure 1-3. Therefore, the DDFS method of constructing a signal is almost entirely digital, and the precise amplitude, frequency, and phase are known and controlled at all times. For these reasons, the switching speed is extremely high, but the power consumption could be excessive at high clock frequencies. The DDFS method is not entirely digital in the true sense of the word since it requires a DAC and a low-pass filter (LPF) to attenuate spurious frequencies produced by the digital switching. In addition, a very stable frequency reference clock of at least three times the output frequency is required. Considering this and the fact that the DAC and LPF might be difficult to build and would consume excessive amount of power at gigahertz operational frequency, the DDFS solution is not acceptable for radio-frequency (RF) applications such as mobile communication terminals.

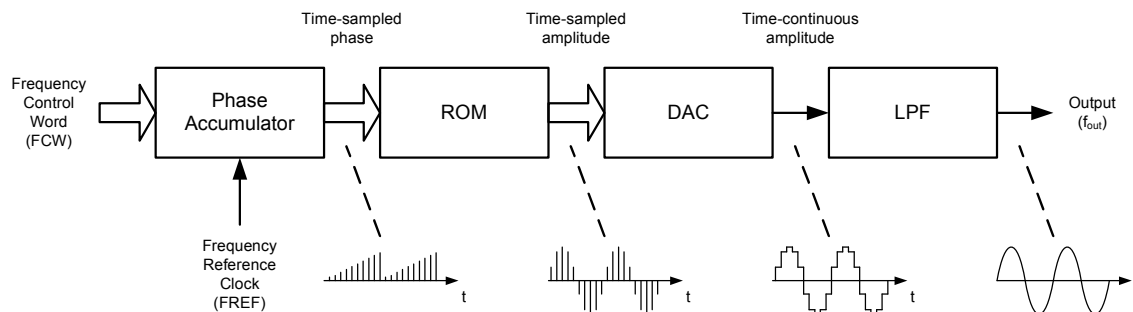


Figure 1-3 Direct digital frequency synthesis [Tierney 71].

Due to its digital waveform reconstruction nature, the DDFS technique is best suited for implementing wideband transmit modulation as well as fast channel hopping schemes [Tan 95]. As an example, Figure 1-4 shows the phase accumulator front end of a DDFS system