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FACULTY OF ENGINEERING
CAIRO – EGYPT

RF Power Amplifier for high bit rate LEO Satellite Transmitter

A Thesis

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STATEMENT

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The work included in this thesis was carried out by the author in the Department of Electronics and Communications Engineering, Ain Shams University.

No part of this Thesis has been submitted for a degree or a qualification at any other university or institute.

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RF Power Amplifier for high bit rate LEO Satellite Transmitter

Abstract

Power amplifiers are key component in the transmitting end of nearly every communication system. The design of the power amplifier (PA) aims to fulfill a number of specifications such as achieving good linearity, acceptable power added efficiency and low power consumption. The PA design requirements include good input and output impedance matching over the operating band of frequency, good reverse isolation and high flat gain. To eliminate the harmonics generated by the nonlinearity of power amplifier and transmitting only the required signal, a low pass filter is used after the PA. The proposed power amplifier has been designed to work for Low Earth Orbit (LEO) satellites. Such satellites usually operate in the X-band of the microwave frequency spectrum.

This thesis focuses on the design of a three stage PA. The three stages PA operates from 8 to 12 GHz. The first stage consists of a cascaded inductive degeneration common source structure designed for maximum gain while the second and third stages are a simple common source topology designed for maximum power added efficiency. The proposed PA achieves 17 ~ 18 dB power gain with a good input matching ($S_{11} < -8$ dB), a good output matching ($S_{22} < -10$ dB), and the average value of power added efficiency (PAE) when the input power 5 dBm is 50% over the 4-GHz bandwidth (from 8 GHz to 12 GHz). The total power consumption of the PA is 0.24 W from 2.5 V supply voltage. Its performance was simulated by using Agilent Advanced Design System (ADS) simulator.

Also this thesis focuses on the design of Butterworth stepped impedance microstrip low pass filter with Defected Ground Structure (DGS). Two filter designs are introduced. The first design is a seventh order low pass filter with three interdigital slots with different finger lengths inserted under the position of high impedance lines. The maximum insertion loss in the passband is better than 0.97 dB and the maximum group delay variation within the passband is less than 10 ps. The other design is a ninth order low pass filter that use different shapes of the DGS (rectangular, square dumbbell and interdigital). The maximum insertion loss is about 0.5 dB and maximum group delay variation is 28 ps. The cutoff frequency of the proposed two designs is 16 GHz. The filter used for LEO satellite application. The filter is analysed using Computer Simulation Technology (CST) Microwave Studio, IE3D zeland and

ADS. The filter is fabricated with photolithographic technique and scattering parameters are measured by using Vector Network Analyzer (VNA) E8719A. Measurements and simulations show good agreement.

Finally the whole system PA plus LPF is analysed using ADS then the whole system is fabricated with photolithographic technique and scattering parameters are measured by using Vector Network Analyzer (VNA) E8719A. The power measurements are made using spectrum analyzer. Measurements and simulations show good agreement.

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