



## DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

### Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE

ın

**Electronics and Communications Engineering** 

### DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

### Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE

in

**Electronics and Communications Engineering** 

Under the Supervision of

Prof. Dr. Ahmed M. Soliman

Dr. Hassan Mostafa

**Emeritus Professor** 

**Assistant Professor** 

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY GIZA, EGYPT 2016

## DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

### Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE

in

Electronics and Communications Engineering

Approved by the
Examining Committee
Prof. Dr. Ahmed M. Soliman, Thesis Main Advisor
Prof. Mohamed Riad, Internal Examiner
Prof. Hassanein H. Amer, External Examiner (Electronics and Communications Engineering, The American University in Cairo)

FACULTY OF ENGINEERING, CAIRO UNIVERSITY GIZA, EGYPT 2016 Engineer's Name: Abdullah Mohamed Ahmed El-Bayoumi

**Date of Birth:** 05/11/1990 **Nationality:** Egyptian

**E-mail:** abdullah.elbayoumi@pg.cu.edu.eg

**Phone:** +20 100 380 7047

**Address:** Electronics and Communications

Engineering Department, Cairo University,

Giza 12613, Egypt

**Registration Date:** 01/10/2012 **Awarding Date:** --/--/2016

**Degree:** Master of Science

**Department:** Electronics and Communications Engineering

**Supervisors:** 

Prof. Dr. Ahmed M. Soliman

Dr. Hassan Mostafa

**Examiners:** 

Prof. Dr. Ahmed M. Soliman (Thesis main advisor)
Prof. Mohamed Riad (Internal examiner)
Prof. Hassanein H. Amer (External examiner)
(Electronics and Communications Engineering, The

American University in Cairo)

#### **Title of Thesis:**

Design of Time-based Analog-to-Digital Converter (T-ADC): High-Performance Variation-Tolerant Differential Voltage-to-Time Converter (VTC) Circuits

#### **Key Words:**

Nanometer CMOS technology; voltage-to-time converter; time-based analog-to-digital converter; software-defined radio; biomedical applications; metal-insulator-metal capacitor; dynamic range.

#### **Summary:**

In this thesis, various metal-insulator-metal (MIM) capacitor-based differential Voltage-to-Time Converters (VTCs) including 2 novel proposed designs, which achieve a high performance at higher sampling frequency for a Software-Defined Radio (SDR) receiver at 65-nm CMOS technology, are presented and compared to their single-ended design. A study on tolerating the process-voltage-temperature (PVT) variations for the 1<sup>st</sup> proposed design with proposing a dynamic calibration technique based on a set of large-sized capacitor-based voltage dividers circuits is presented. Post-layout simulation results are provided for both designs at 130-nm CMOS technology for low-frequency low-power implantable biomedical systems.



### Acknowledgments

To begin with, I would like to take this opportunity by expressing my deepest gratitude and appreciation towards my supervisors Prof. Dr. Ahmed M. Soliman and Dr. Hassan Mostafa. Their continuous support, guidance and enthusiasm have made my research instrumental, intellectually stimulating, enjoyable and very rewarding in successfully performing and completing my thesis. It is a great honor to be accepted as a masters' degree student under the supervision of Prof. Dr. Soliman. It is really remarkable to attend the IEEE International Conference on Electronics, Circuits and Systems (ICECS 2015) as an author and watch the honorary ceremony of Prof. Dr. Soliman for his amazing research contribution record in the cutting-edge technologies for academia and industry. His inspiration stories and his excellence dedication have guided me to finalize this work.

Also, I would like to specialize my thanks to Dr. Mostafa who has shaped my research direction with his ideas. His vision, mentorship, professional advices of technical and non-technical issues and friendship have advanced me through the thesis, although his lots of postgraduate and undergraduate students. These also encourage me to take the lead and participate in various international conferences. That helps me to get accepted of some of them. As we know the main aspect of any journey is to understand your failures, I have learnt from Dr. Mostafa to study well the review comments of my rejected papers and analyze them to start again. I really appreciate Dr. Mostafa's patience towards me regarding the work load of my industrial career. I am also thankful to Dr. Mohamed Refky for using his experience and knowledge to help me whenever I needed it. I would like to thank my fellow graduate students in the EECE department who have provided me with the tools and support needed to complete this dissertation.

Research is something when you change your way of thinking. This process of change may be slow. Thus, it could leave you completely unaware of the change you have made, and the progress that you are currently making. An instance of recollection, such as writing a summary of the progress you have been doing for the last years brings these things to your attention. This process of change is something that your environment is aware of, as one is thrown between despair and hope. Being a software engineer in a multinational company is stressful and at times it is emotionally challenging to struggle to manage your time between your industrial work background and your academic research. Although, they could fulfill a perfection background of how we innovate ideas till we can provide products to the market. Finally, I am also grateful to all my friends who have encouraged me to keep going on and brought social balance into my life.

### **Dedication**

I have devoted this dissertation with a special thank you to my family for helping me to come this far and for being a continuous source of love, care, warmth and stability throughout my life. Collectively, they are an enormous pool of support for which I would not have succeeded without. I owe them every single achievement in my life.

## **Table of Contents**

ACKNOWLEDGMENTS	I
DEDICATION	II
TABLE OF CONTENTS	III
LIST OF TABLES	VII
LIST OF FIGURES	IX
NOMENCLATURE	XII
LIST OF PUBLICATIONS	XIV
ABSTRACT	XV
CHAPTER 1: INTRODUCTION	1
1.1. MOTIVATION	2
1.2. Thesis scope	
1.3. THESIS OVERVIEW	
CHAPTER 2 : LITERATURE REVIEW	
2.1. ANALOG-TO-DIGITAL CONVERTER	
2.1.1. SAMPLING	
2.1.2. QUANTIZATION	
2.2. ADC TYPES	
2.2.1. DIRECT CONVERSION ADCS	
2.2.1.1. NYQUIST-RATE ADC	
2.2.1.1.1. SUCCESSIVE-APPROXIMATIO	N ADC9
2.2.1.1.2. FLASH ADC	10
2.2.1.1.3. PIPELINED ADC	12
2.2.1.1.4. TIME-INTERLEAVED ADC	14
2.2.1.2. OVERSAMPLING ADC	15
2.2.1.2.1. SIGMA-DELTA MODULATOR	15
2.2.2. INDIRECT CONVERSION ADCS	17
2.2.2.1. NYQUIST-RATE ADC	17
2.2.2.1.1. INTEGRATING-BASED ADC	17
2.2.2.2. OVERSAMPLING ADC	18
2.2.2.2.1. PWM-BASED ADC	18

2.2.2.2.2	. VTC-BASED ADC	19
2.2.2.3	. VCO-BASED ADC	19
2.3.	PERFORMANCE METRICS	20
2.3.1.	ADC CHARACTERISTICS	20
2.3.1.1.	GAIN ERROR	20
2.3.1.2.	OFFSET ERROR	20
2.3.1.3.	INTEGRAL NON-LINEARITY	21
2.3.1.4.	DIFFERENTIAL NON-LINEARITY	22
2.3.1.5.	MISSING CODES	23
2.3.2.	VTC CHARACTERISTICS	23
2.3.2.1.	LINEARITY AND DYNAMIC RANGE	23
2.3.2.2.	VOLTAGE SENSITIVITY	24
2.3.2.3.	MAXIMUM SAMPLING FREQUENCY	24
2.3.2.4.	TOTAL HARMONIC DISTORTION	24
2.3.2.5.	SIGNAL-TO-NOISE-AND-DISTORTION RATIO	25
2.3.2.6.	EFFECTIVE NUMBER OF BITS	25
2.3.2.7.	RESOLUTION	25
2.3.2.8.	NOISE	25
2.3.2.9.	AREA	26
2.3.2.10.	POWER	26
2.3.2.11.	FIGURE-OF-MERIT	26
_	ER 3 : NOVEL DIFFERENTIAL VTC CIRCUITS FOR HIGH-SI	
3.1. 3.2.	INTRODUCTION	
3.2.1.	THE DIFFERENTIAL FALLING VTC DESIGN	30
3.2.2.	SIMULATION RESULTS	32
3.3.	DIFFERENTIAL RISING VTC CIRCUIT	34
3.3.1.	THE DIFFERENTIAL RISING VTC DESIGN	34
3.3.2.	SIMULATION RESULTS	35
3.4.	DIFFERENTIAL VTC METHODOLOGY CIRCUIT	36
3.4.1.	THE DIFFERENTIAL VTC METHODOLOGY DESIGN	36

3.4.2.	SIMULATION RESULTS	38
3.5.	MODIFIED DIFFERENTIAL VTC METHODOLOGY CIRCUIT	40
3.5.1.	THE 1ST DIFFERENTIAL VTC PROPOSED DESIGN	40
3.5.2.	SIMULATION RESULTS	42
3.5.3.	PVT VARIATIONS CALIBRATION	45
3.5.3.1	. PROCESS VARIATIONS	46
3.5.3.1	.1. BEFORE CALIBRATION	46
3.5.3.1	.2. AFTER CALIBRATION	48
3.5.3.2	. VOLTAGE VARIATIONS	51
3.5.3.2	.1. BEFORE CALIBRATION	51
3.5.3.2	.2. AFTER CALIBRATION	54
3.5.3.3	. TEMPERATURE VARIATIONS	57
3.5.3.3	.1. BEFORE CALIBRATION	57
3.5.3.3	2.2. AFTER CALIBRATION	60
3.5.4.	MIMCAP-BASED DESIGN VERSUS MOSCAP-BASED DESIGN	63
3.6.	DIFFERENTIAL HIGH-SPEED VTC CIRCUIT	63
3.6.1.	THE 2 <sup>ND</sup> DIFFERENTIAL VTC PROPOSED DESIGN	63
3.6.2.	SIMULATION RESULTS	64
СНАР	TER 4: DIFFERENTIAL VTC CIRCUITS FOR HIGH-ACCURACY	
BIOM	EDICAL APPLICATIONS	67
4.1.	Introduction	67
4.2.	MODIFIED DIFFERENTIAL VTC METHODOLOGY CIRCUIT AT 130-NM CMOS.	68
4.2.1.	POST-LAYOUT RESULTS WITHOUT THE CALIBRATION	
CIRC	UIT	68
4.2.2.	POST-LAYOUT RESULTS WITH THE CALIBRATION CIRCUIT	74
4.3.	DIFFERENTIAL HIGH-SPEED VTC CIRCUIT AT 130-NM CMOS	77
DISCU	USSION AND CONCLUSIONS	81
1.	PROPOSED DESIGNS PERFORMANCE	81
2.	FUTURE WORK	81
3.	CONCLUSION	83
REFE	RENCES	84
APPE	NDIX A: DESIGN PARAMETERS	88
A.1	DIFFERENTIAL FALLING VTC DESIGN PARAMETERS AT 65-NM CMOS	88

A.2	DIFFERENTIAL RISING VTC DESIGN PARAMETERS AT 65-NM CMOS	88
A.3	DIFFERENTIAL VTC METHODOLOGY DESIGN PARAMETERS AT 65-NM CMO	S 89
A.4	MODIFIED DIFFERENTIAL VTC METHODOLOGY DESIGN PARAMETERS AT	65-
NM C	MOS	89
A.5	DIFFERENTIAL HIGH-SPEED VTC DESIGN PARAMETERS AT 65-NM CMOS	90
A.6	DIFFERENTIAL VTC METHODOLOGY DESIGN PARAMETERS AT 130-NM CM	OS 92
A.7	DIFFERENTIAL HIGH-SPEED VTC DESIGN PARAMETERS AT 130-NM CMOS	92
APPEN	NDIX B: SIMULATIONS METHODS	94
B.1	LINEARITY CHECK	94
B.2	CIRCUIT SENSITIVITY	
B.3	TOTAL HARMONIC DISTORTION	102
B.4	POWER CONSUMPTION	
B.5	Noise Figure	105
B.6	EFFECTIVE NUMBER OF BITS	107
B.7	PVT VARIATIONS	115

## **List of Tables**

Table 2.1: ADC resolution and sampling rate for various applications24
Table 3.1: Performance comparison between the differential falling VTC circuit and its single-ended design @ 3% linearity error
Table 3.2: Performance comparison of the differential falling while sweeping the
sampling frequency with a 3% linearity error.
Table 3.3: Performance comparison between the differential rising VTC circuit and its
single-ended design @ 3% linearity error35
Table 3.4: Performance comparison between the differential VTC methodology circuit
and its single-ended design @ 3% linearity error39
Table 3.5: Performance comparison of the differential methodology while sweeping the
sampling frequency with a 3% linearity error
Table 3.6: Performance comparison between the modified differential VTC
methodology circuit and its single-ended design @ 3% linearity error44
Table 3.7: Performance comparison before calibration between the proposed design and
the single-ended design at different corners47
Table 3.8: Performance comparison after calibration between the proposed design and
the single-ended design at different corners
Table 3.9: Performance comparison before calibration between the proposed design and
the single-ended design at supply voltage variations53
Table 3.10: Performance comparison after calibration between the proposed design and
the single-ended design at supply voltage variations
Table 3.11: Performance comparison before calibration between the proposed design
and the single-ended design at temperature variations57
Table 3.12: Performance comparison after calibration between the proposed design and
the single-ended design at temperature variations60
Table 3.13: Performance comparison between the proposed design with a MIMCAP
and a MOSCAP at a fixed dynamic range and DC bias voltage63
Table 3.14: Performance comparison between the differential high-speed VTC circuit
and its single-ended design @ 3% linearity error66
Table 3.15: Performance comparison of the single-ended high-speed VTC while
sweeping the sampling frequency
Table 3.16: Performance comparison of the differential high-speed VTC while
sweeping the sampling frequency
Table 4.1: Post-layout performance comparison between the 1 <sup>st</sup> proposed design and its
single-ended VTC circuit at 3 % linearity error
Table 4.2: Post-layout performance comparison of the 1 <sup>st</sup> proposed design corner
variations at 3 % linearity error before calibration74
Table 4.3: Post-layout performance comparison of the 1 <sup>st</sup> proposed design corner
variations at 3 % linearity error after calibration
Table 4.4: Post-layout performance comparison between the 2 <sup>nd</sup> proposed design and its
single-ended VTC circuit
Table A.1: Design parameters of the core of the differential falling VTC circuit88
Table A.2: Design parameters of the core of the differential rising VTC circuit88

Table A.3: Design parameters of the XNOR gate of the single core of the differential
VTC methodology circuit89
Table A.4: Design parameters of the output inverter of the single core of the differential
VTC methodology circuit89
Table A.5: Design parameters of the modified differential VTC methodology circuit. 90
Table A.6: Design parameters of the set of the calibration circuits on PVT variations. 90
Table A.7: Design parameters of the single core of the differential high-speed VTC
circuit91
Table A.8: Design parameters of the single core of the 1 <sup>st</sup> proposed differential VTC
circuit91
Table A.9: Design parameters of the set of the calibration circuits on PVT variations. 92
Table A.10: Design parameters of the single core of the 2 <sup>nd</sup> proposed VTC circuit93

# **List of Figures**

Figure 1.1: TADC architecture	2
Figure 2.1: A functionality of a 3-bit ADC	6
Figure 2.2: An input signal spectrum achieving the Nyquist-rate criterion	
Figure 2.3: An input signal spectrum not achieving the Nyquist-rate criterion	
Figure 2.4: Original signal versus quantized signal	
Figure 2.5: Quantization error representation	
Figure 2.6: SAR architecture	
Figure 2.7: SAR algorithm	
Figure 2.8: Flash ADC architecture	
Figure 2.9: Folded flash ADC architecture	
Figure 2.10: Pipeline ADC architecture	
Figure 2.11: Block diagram of a single stage of a pipeline ADC	
Figure 2.12: Cyclic ADC architecture	
Figure 2.13: Time-interleaved ADC architecture	
Figure 2.14: First-order $\Sigma\Delta$ ADC architecture. (a) error feedback model. (b) output	
feedback model	
Figure 2.15: Second-order $\Sigma\Delta$ ADC architecture	
Figure 2.16: Single-slope ADC architecture	
Figure 2.17: Dual-slope ADC architecture	
Figure 2.18: PWM based ADC architecture	
Figure 2.19: ADC gain error	
Figure 2.20: ADC offset error	
Figure 2.21: ADC integral non-linearity	
Figure 2.22: ADC differential non-linearity	
Figure 2.23: ADC missing code output	23
Figure 3.1: Smartphone receiver chains.	27
Figure 3.2: Software defined radio receiver block diagram.	
Figure 3.3: The differential VTC architecture	
Figure 3.4: Circuit schematic of the core of a differential falling VTC circuit	
Figure 3.5: VTC operation mode timing diagram.	
Figure 3.6: Differential falling VTC. (a) Linear range at $F_S = 250$ MS/s. (b) Linearity	y
error check at $F_S = 250$ MS/s. (c) Linear range at $F_{S,MAX} = 4$ GS/s. (d) Linearity error	r
check at $F_{S,MAX} = 4 \text{ GS/s}$ .	33
Figure 3.7: Circuit schematic of the core of a differential rising VTC circuit	35
Figure 3.8: Differential rising VTC. (a) Linear range at $F_S = 250$ MS/s. (b) Linearity	
error check at $F_S = 250$ MS/s. (c) Linear range at $F_{S,MAX} = 0.7$ GS/s. (d) Linearity error check at $F_S = 250$ MS/s.	or
check at $F_{S,MAX} = 0.7 \text{ GS/s}$	36
Figure 3.9: The differential methodology architecture	37
Figure 3.10: The VTC core of the differential methodology architecture	37
Figure 3.11: The XNOR circuit schematic.	
Figure 3.12: Differential VTC methodology. (a) Linear range at $F_S = 250$ MS/s. (b)	
Linearity error check at $F_S = 250$ MS/s. (c) Linear range at $F_{S,MAX} = 2.5$ GS/s. (d)	
Linearity error check at F <sub>S,MAX</sub> = 2.5 GS/s.	
Figure 3.13: The proposed modified differential methodology architecture	41

Figure 3.14: The modified differential VTC methodology design. (a) Dynamic linear
range (b) Linearity error check
Figure 3.15: The single-ended VTC core. (a) Dynamic linear range (b) Linearity error check
Figure 3.16: The calibration circuit integrated with the proposed design45
Figure 3.17: The proposed differential VTC before calibration at worst-case corners
variations. (a) Dynamic linear range (b) Linearity error check47
Figure 3.18: The single-ended VTC core before calibration at worst-case corners
variations. (a) Dynamic linear range (b) Linearity error check48
Figure 3.19: The proposed differential VTC after calibration at worst-case corners
variations. (a) Dynamic linear range (b) Linearity error check49
Figure 3.20: The single-ended VTC core after calibration at worst-case corners
variations. (a) Dynamic linear range (b) Linearity error check51
Figure 3.21: The proposed differential VTC before calibration at voltage variations. (a)
Dynamic linear range (b) Linearity error check
Figure 3.22: The single-ended VTC core before calibration at voltage variations. (a)
Dynamic linear range (b) Linearity error check
Figure 3.23: The proposed differential VTC after calibration at voltage variations. (a)
Dynamic linear range (b) Linearity error check
Figure 3.24: The single-ended VTC core after calibration at voltage variations. (a)
Dynamic linear range (b) Linearity error check56
Figure 3.25: The proposed differential VTC before calibration at temperature
variations. (a) Dynamic linear range (b) Linearity error check58
Figure 3.26: The single-ended VTC core before calibration at temperature variations.
(a) Dynamic linear range (b) Linearity error check
Figure 3.27: The proposed differential VTC after calibration at temperature variations.
(a) Dynamic linear range (b) Linearity error check61
Figure 3.28: The single-ended VTC core after calibration at temperature variations. (a)
Dynamic linear range (b) Linearity error check62
Figure 3.29: Circuit schematic of the core of the differential high-speed VTC design. 64
Figure 3.30: Curve fitting of the linear range using MATLAB. (a) The 2 <sup>nd</sup> proposed
differential VTC design. (b) The single-ended design65
Figure 3.31: Linearity error check of the linear range using MATLAB. (a) The 2 <sup>nd</sup>
proposed differential VTC design. (b) The single-ended VTC design65
Figure 4.1: Layout of the 1 <sup>st</sup> proposed VTC design68
Figure 4.2: The post-layout linear range of the 1 <sup>st</sup> proposed VTC design at 3 % linearity
error69
Figure 4.3: The post-layout linear range with the DC bias of the single-core of the 1 <sup>st</sup>
proposed VTC design at 3 % linearity error69
Figure 4.4: The post-layout linearity error check of the 1st proposed VTC design70
Figure 4.5: The post-layout linearity error check of the single-core of the 1 <sup>st</sup> proposed
VTC design
Figure 4.6: Dynamic range of the 1 <sup>st</sup> proposed differential VTC at SS corner before
calibration at 3% linearity error
Figure 4.7: Linearity error check of the 1 <sup>st</sup> proposed differential VTC at SS corner
before calibration
Figure 4.8: Linearity error check of the 1 <sup>st</sup> proposed differential VTC at FF corner72
Figure 4.9: Linearity error check of the 1 <sup>st</sup> proposed differential VTC at FF corner73

Figure 4.10: Dynamic range of the 1 <sup>st</sup> proposed differential VTC at SS corner after	
calibration at 3% linearity error.	75
Figure 4.11: Linearity error check of the 1st proposed differential VTC at SS corner	
after calibration	
Figure 4.12: Layout of the 2 <sup>nd</sup> proposed VTC design	
Figure 4.13: The post-layout linear range of the 2 <sup>nd</sup> proposed VTC design at allowed	d
linearity error.	78
Figure 4.14: The post-layout linear range of the single-core of the 2 <sup>nd</sup> proposed VTO	
design at allowed linearity error.	
Figure 4.15: The post-layout linearity error check of the 2 <sup>nd</sup> proposed VTC design	
Figure 4.16: The post-layout linearity error check of the single-core of the 2 <sup>nd</sup> propo	
VTC design.	
Figure B.1: Choosing the DC analysis on Virtuoso Analog Design Environment	94
Figure B.2: Choosing the transient analysis on Virtuoso ADE	
Figure B.3: Adding the design variables on Virtuoso ADE	
Figure B.4: Opening the Virtuoso Calculator	
Figure B.5: Delay equation on Virtuoso Calculator	
Figure B.6: Outputs on Virtuoso ADE.	
Figure B.7: Outputting the Delay equation on Virtuoso ADE	
Figure B.8: Parametric Analysis on Virtuoso ADE.	
Figure B.9: Sweeping the input voltage.	
Figure B.10: Starting drawing the delay equation	
Figure B.11: The VTC dynamic linear range	
Figure B.12: Delay buffer calculation.	
Figure B.13: CSV saved file	
Figure B.14: Circuit sensitivity.	
Figure B.15: DFT on Virtuoso Calculator	.103
Figure B.16: Power configuration on Virtuoso ADE	.104
Figure B.17: Current configuration on Virtuoso ADE	
Figure B.18: Power equation on Virtuoso Calculator.	
Figure B.19: Noise analysis configuration on Virtuoso ADE	.106
Figure B.20: Noise expression on Virtuoso ADE.	
Figure B.21: Model libraries setup on Virtuoso ADE	
Figure B.22: Modifying the device model process	
Figure B.23: Temperature libraries setup on Virtuoso ADE	
Figure B.24: The operating temperature setup on Virtuoso ADE	.116