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# Functionality Improvement of SDH Multiplexer In Backbone Transmission Networks

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# Abstract

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This dissertation presents a study of synchronous digital hierarchy multiplexers as part of backbone transmission networks. The study is presented through the terminal multiplexer with data rate 155 Mbit/s.

Chapter1 begins with an introduction to the different transmission systems, starting from the pulse code modulation (PCM) and the conversion from analog to digital to have digital signal. The conversion process is implemented by different global systems, where the American system uses the **μ-Law** and the European system uses **A-law**. The two transmission systems produce the 1.5 Mbit/s for American system and 2.048 Mbit/s for European system in the transmission networks.

Chapter 2 concentrates in the European transmission system which is widely used in the most of countries. A study of the plesiochronous digital hierarchy (PDH) transmission system is introduced in more details, the study indicates the multiplexing process through the PDH system and how it uses **bit by bit** multiplexing with different clock sources. Uses this type of the multiplexing process makes the PDH system limited in the management and the monitoring system, in addition restricted it in the highest bit rates of the multiplexing process, where the highest bit rate in the PDH system is 565 Mbit/s.

Chapter 3 introduces a study of the synchronous transmission system (SDH) is presented in more details, this by understanding the frame structure and the bytes descriptions of the SDH frame. The multiplexing process of the SDH system uses **byte by byte** multiplexing with centralized clock source , this type of the multiplexing process makes the SDH system more advanced in the management and monitoring systems, also the highest bit rates of the multiplexing process reached to 40 Gbit/s. The STM1 frame was taken as example of the PDH signal. Next the deference types of the SDH multiplexers with the connection topologies are introduced.

Chapter 4 illustrates the different types of the SDH multiplexers and the network topology of it.

In chapter 5 a simulation of the terminal multiplexer C based was presented. The simulation indicates the multiplexing process of the terminal multiplexer by combining 63 × 2.048 Mbit/s to form the 155 Mbit/s (STM-1) frame. In addition, the descriptions of the SOH bytes are discussed. In addition, the measurement tool is

used as Matlab Model and there is compassion between the output of the C model and the matlab output.

Chapter 6 introduces the conclusion of the thesis . In the STM-1 frame for example, there are 41 bytes in the section overhead not used or reserved for future. This is means that there is a bandwidth 1.6% of the total bandwidth not used or 2.64 Mbit/sec wasted. From the study, by using the C programming language and after implementing the model using FPGA , it can help in understanding the available resources of the transmission networks in the telecommunication companies and how it can be used in a professional ways. The model of the STM-1 terminal multiplexer can help in many R&D centres inside our country to develop a new model of the SDH multiplexers with more functions and more features.

**Key words:** Byte by Byte Multiplexing, Bit by Bit multiplexing, terminal multiplexer, Section Overhead (SOH), Path Overhead (POH), 2 Mbit/s, 155 Mbit/s.

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# *List of Abbreviations*

| | |
|---|---|
| **A/D** | Analog to Digital Converter |
| **ADM** | Add/Drop Multiplexer |
| **AIS** | Alarm Indication Signal |
| **ATM** | *Asynchronous Transfer Mode* |
| **AU** | Administrative Unit |
| **BBE** | *Background Blocked Errors* |
| **BIP** | Bit Interleaved Parity |
| **BLSR** | Bidirectional Line Switched Ring |
| **C-N** | Container of Order N |
| **CAS** | Channel Associated Signal |
| **CEPT** | European Conference of Postal and Telecommunications Administrations |
| **CRC** | *cyclic redundancy check* |
| **D/A** | Digital to Analog Converter |
| **E1** | Digital data signal with bit rate 2.048Mbit/s |
| **FAS** | Frame Alignment Signal |
| **GSM** | *Global System for Mobile* Communications |
| **ITU** | International Telecommunication Union |
| **MS** | Multiplex Section |
| **MSOH** | Multiplex Section Overhead |
| **NFAS** | Not Frame Alignment Signal |
| **OAM** | Operation, Administration and Maintenance |
| **PAM** | Pulse Amplitude Modulation |
| **PCM** | Pulse Code Modulation |
| **PDH** | Plesiochronous Digital Hierarchy |
| **PNTR** | Pointer |
| **POH** | Path Over Head |
| **PRC** | primary reference clock |
| **PTE** | Path Termination Element |
| **RDI** | Remote Defect Indication |

**REG** Regenerator
**SAN** Storage Area Network
**SDH** Synchronous Digital Hierarchy
**SEC** Synchronous Equipment Timing Clock
**SEMF** Synchronous Equipment Management Function
**SNCP** Subnetwork Connection Protection
**SNR** The Signal to Noise Ratio
**SOH** Section Over Head
**SONET** Synchronous Optical Network
**STM-1** Synchronous Transport Module Level-1
**TU** Tributary Unit
**UPSR** Unidirectional Path Switched Ring
**USA** *United States of America*
**VC** Virtual Container

# *Chapter 1*
# *Introduction*

## 1.1 Thesis motivation

Due to the competitions between the telecommunication service providers, the required capacities are increasing all the time. It is important for these providers to develop a network that can transfer more data bytes from one place to another. In addition, The GSM traffic and the internet services need more capacities in the telecommunication networks. Therefore, it is mandatory for the networks to handle large amounts of data in a fast and a reliable ways. Of course, one possibility would be Ethernet traffic, but in cellular transmission networks there are a strict requirements for delay, data loss and synchronization and this is why the Ethernet is not yet supported.

The Synchronous Digital Hierarchy (SDH) is one answer for increasing the network data traffic. For example if we need to transfer 63 × 2.048 Mb/s (E1) signals from one place to another a huge amount of wires will be needed, on the other hand the SDH needs only two fibers to do the same operation. Many vendors have a product called STM1 multiplexer and its functionality to add and drop 63 × 2.048 Mbit/s into 155.52 Mbit/s (STM-1).

The bit rates of the basic signals in the SDH are derived from the same clock source, which means that the SDH is completely synchronous transmission system. SDH has many different hierarchy levels starting from 155.52 Mbit/s to 10 Gbit/s and the STM-1 with a bit rate of 155.52 Mbit/s is the basic module of the SDH system. The SDH signal is terminated to E1 (2.048 Mbit/s) signals by using terminal multiplexer.

Before the SDH multiplexer operates in the telecommunication market, there is a huge amount of work to put the requirements specifications, by studying the reality of the market needs. Many chip manufacturers have SDH chips in their product catalog, so one has to make a decision which manufacturer's chip to use. In addition, one must decide how to handle overhead bytes and how to implement all this in network manager software. After all these decisions, we have a huge amount of data and the last thing to do is to decide which features are implemented and which are not. Because of time-to-market pressures, the implementation has to be phased and the first phase must contain only the necessary functionality and nothing more to reduce the development time to minimum.

The Synchronous Digital Hierarchy (SDH) multiplexers form the core part of the backbone telecommunication networks, and the effective design, reliability analysis and training are essential to managing SDH network effectively.

This thesis studies an implementation design of the SDH multiplexer by C programming language. The design is implemented according to International Telecommunication Union (ITU-T) standards. It doesn't cover all aspects of the wide range of the SDH adaptations.

## 1.2 Thesis Overview

This thesis is organized in six chapters. Chapter 2 introduces the existing transmission systems. It includes an overview of pulse code modulation (PCM), 2.048 Mbit/s frame and plesiochronous digital hierarchy (PDH) transmission system.

Chapter 3 presents a full description of the synchronous digital hierarchy (SDH) transmission system; it shows the advantages of the SDH, general frame structure of the SDH and the STM1 frame format.

The different types of the SDH multiplexers and the networks topology are described in chapter 4. In addition, it contains a brief description of the management system.

Chapter 5 presents an implementated model of SDH terminal multiplexer by using C programming language with a flowchart of the C code and the tests of the model are explained at the end of the chapter.

Chapter 6 provides the conclusion and the future work.