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Sigma Delta Analog to Digital Converters For Wireless Receivers

A Thesis

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Abstract

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This thesis presents low-voltage, low-power system and circuit design techniques of high linearity discrete time sigma delta modulators. The target application is analog to digital conversion in wireless receivers with wide channel bandwidths implemented in DSM (deep sub-micron) CMOS technologies.

On the system level, a sigma delta modulator with *relaxed analog requirements* is proposed. It is based on multibit quantization and a hybrid of feedforward and feedback loop filter architectures with input signal feed-in at critical nodes. This architecture facilitated the use of low gain, power efficient telescopic OTAs (operational transconductance amplifiers) in the loop filter at a low supply voltage of 1.2V.

On the circuit level, a low voltage, low power implementation of the high linearity input feedforward modulator architecture is proposed with a new clocking scheme that reduces the timing complexity in the feedback path. The implementation avoids both the power hungry, nonlinear active solutions and the severe signal attenuation of passive ones.

The research also shows that *digitally assisted analog processing* is an attractive low power alternative in DSM technologies, where DEM (dynamic element matching) was used to relax the matching requirements of the feedback DAC capacitors. A power efficient implementation of the DWA (data weighted averaging) algorithm is presented and designed.

The effect of process variations on the performance of SC (switched capacitor) circuits was investigated. It is shown that significant power savings can be achieved by controlling the dynamics of the amplifiers at the core of any SC circuit over process. Toward that end, a biasing scheme is proposed that achieves constant slew rate and constant gain bandwidth product across process corners.

A top down design methodology was followed to implement the proposed switched capacitor sigma delta modulator in a $0.13\mu\text{m}$ CMOS process. The modulator achieves an ENOB of 14-bit with more than 110dB SFDR over the WCDMA channel bandwidth of 1.92 MHz at an oversampling ratio of 20X, while consuming a worst case current of

3.85mA from a 1.2V supply for both the analog and the digital parts. This resulted in a FOM (figure of merit) of $73fJ/Conversion$, outperforming the state of the art continuous time and discrete time sigma delta modulators.

Key words: Sigma Delta modulator, Input signal feedforward, Process variations, Reduced analog requirements, Digitally assisted analog processing, constant slew rate and constant gain bandwidth product biasing.

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