



**AIN SHAMS UNIVERSITY**  
**FACULTY OF ENGINEERING**

**Electronics and Communications Department**

# **Interface Circuits Design for piezo- resistive Sensors**

A Thesis submitted in partial fulfillment of the requirements of  
a Master of Science degree in Electrical Engineering  
Electronics Engineering and Electrical Communications Department

by

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**Faculty of Engineering Ain Shams University**  
**Electronics and Communication Engineering**  
**Department**

**Thesis title: "Interface Circuits Design for piezo-resistive Sensors"**

**Submitted by: Amr Walid Saad Eldain**

**Degree: Master of Science in Electrical Engineering**

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# Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

**Amr Walid Saad Eldain Hassan**

Signature

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**Date:** 1/6/2016



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# Abstract

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## **Abstract**

In the recent years, there has been a growing demand on high resolution pressure sensors for new applications such as mobile altimeter, air speed measurements, control systems, medical instruments and accuracy enhancement of the GPS receivers. Many of these applications are hand-held or battery operated, therefore the power dissipation of the pressure sensors remains as a main concern. In piezo-resistive sensors, the pressure to be measured changes the resistance value of piezo-resistive element. Typically, piezo-resistive sensors are realized in one of two configurations, either as a single resistor with current excitation, or in the form of

Wheatstone bridge. Although a single resistor configuration can potentially achieve high signal-to-noise ratio (SNR), the Wheatstone bridge is the most widely used readout configuration, due to its implementation simplicity and its immunity to common mode noise and interference from supply and environmental disturbance such as temperature, which in turn relax the interface circuit design.

Compared to capacitive pressure sensors, piezo-resistive pressure sensors consume dc current in the sensor itself, making resistive sensors less attractive for low-power applications. The objective of this work is to extend the applications of piezo-resistive sensors to the low power domain. The proposed interface circuit is different than conventional interface circuits by periodically switch the resistive bridge to save power. To reduce the interface circuit power even further, the turn ON time of different system blocks is optimized. The proposed interface is composed of a sample-and-hold circuit, a front-end-amplifier and a  $\Delta\Sigma$  analog-to-digital-converter. The proposed interface is implemented in  $0.13\mu m$  standard CMOS technology with  $1.2V$  supply voltage. The interface circuit achieves a high resolution of 13.82 bits with  $221.8\mu W$  as a total power consumption, including the bridge power. Hence, a very low figure-of-merit of  $5.076 \text{ pJ/Conversion}$  is attained.

Keywords: Pressure sensor, low power interface circuit, low power Wheatstone bridge, resistive pressure sensor, delta-sigma ( $\Delta\Sigma$ ) modulator, incremental A/D converter

# Thesis Summary

## Summary

The thesis is divided into five chapters as listed below:

### Chapter 1

Gives a solid background, motivation, and objective for this work is presented reaching the adoption of an application for the proposed resistive interface. The chapter ends with a brief summary for the thesis organization.

### Chapter 2

An overview on piezo-resistive pressure sensing systems is presented and the principle of operation of pressure sensor devices is explained. Also, advantages and disadvantages of every architecture are discussed.

### Chapter 3

A new interface architecture for piezo-resistive pressure sensors is proposed. System block diagram is introduced where all system sub-blocks are highlighted.

### Chapter 4

Presents the circuit level implementation of the proposed system. Analysis, design steps, and simulation results of the sub-blocks are presented. Finally the proposed interface system performance is compared with the state-of-the-art interfaces.

Chapter 5

The conclusion of this thesis is listed and discussed.

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