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Graph-Based Approach for Symmetry Detection

A Thesis

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Submitted by

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STATEMENT

This Thesis is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of Computer and Systems Engineering, Ain Shams University.

No part of this Thesis has been submitted for a degree or a qualification at any other university or institute.

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ABSTRACT

Symmetry detection plays an important role in many applications. One of those applications is detecting symmetries of the Integrated Circuits layouts. Symmetry can be presented excessively in one layout design as it provides high efficiency in the circuit performance. Maintaining the geometrical symmetry of the circuit components during the layout compaction has great impact on analog circuit performance and poses great challenges to analog layout automation. Device matching and symmetry are very important in layout design of high performance analog circuits. The aim of this thesis is to find an efficient solution for detecting symmetry in Integrated Circuits layout. Approaches used to detect IC layout symmetry depend on extracting information from the circuit design. A new approach is presented to detect IC layout symmetry between polygons using image processing. In this thesis, a novel method for detecting symmetry is introduced. Taking advantage of the type of images used of layout designs to have more efficient symmetry detection algorithm.

The algorithm is implemented by C++ and tested using several analog layout designs. The new algorithm is successful in detecting symmetry in layout images compared to other ones. This approach detects translation, scale, rotation and partial symmetries in the IC layout design. In comparison to famous symmetry detection algorithms like SIFT, the new approach succeeds to detect symmetric polygons with higher speed and more accurate results.

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Contents

List of Figures	XI
List of Tables	XIII
List of Abbreviations	XVI
List of Symbols	XVII
1 Introduction	1
1.1 Motivation	2
1.2 Problem statement	2
1.3 Thesis Outline	3
2 Layouts	5
2.1 What is integrated circuit?	5
2.2 Where is layout design from this?	6
2.2.1 Inverter example	7
2.3 Manufacturing overview	8
2.4 Layout design rules	10
2.4.1 Scalable design rules	12
2.5 Symmetry in layout	13
2.5.1 Levels of symmetry	14

CONTENTS

2.5.1.1	Inter-device symmetry	14
2.5.1.2	Intra device symmetry	15
2.5.1.3	Bulk symmetry	16
2.5.1.4	Routing Symmetry	17
2.6	Layout automation	19
2.6.1	Analog layout automation approaches	19
3	Symmetry detection approaches	23
3.1	Introduction	23
3.2	Description	26
3.2.1	Gradient-based symmetry detectors	26
3.2.1.1	Methodology	26
3.2.1.2	Disadvantages	27
3.2.2	Phase-based symmetry detectors:	27
3.2.2.1	Advantages	29
3.2.2.2	Disadvantages	29
3.2.3	Graph-based symmetry detectors	29
3.3	Feature Extraction	33
3.3.1	Local feature properties	34
3.4	The main flow	35
3.4.1	Feature detectors	36
3.4.1.1	Corner Detectors	37
3.4.1.2	Blob Detectors	38
3.4.1.3	Region Detectors	38
3.4.1.4	Scale-space for feature detectors	38
3.4.1.5	The Gaussian filter and Discrete image convolution	40
3.4.2	Feature descriptors	41
3.4.2.1	SIFT descriptor	41
3.4.2.2	Speeded Up Robust Features SURF	41
3.4.2.3	Gradient location-orientation histogram GLOH	42

CONTENTS

3.4.2.4	An efficient dense descriptor applied to wide-baseline stereo DAISY	42
3.4.3	Feature matching strategies	43
3.4.4	The proposed algorithm	44
4	Feature Extraction	45
4.1	SIFT feature detection	46
4.2	FAST feature detection	50
4.3	HARRIS corner detection	53
4.4	Experiments and results	60
4.4.1	Data set	60
4.4.2	Evaluation of extractors	60
4.5	Conclusion	64
5	Descriptor and Matching	67
5.1	Descriptor	67
5.2	Matching	70
5.2.1	Evaluation of symmetry detection	70
5.2.1.1	The new algorithm results compared to SIFT ones	74
6	Conclusions and Future work	83
A	Fabrication	87
A.1	Introduction	87
A.1.1	The silicon wafer	87
A.1.2	Photolithography	88
A.2	Inverter fabrication example	92
	References	101

CONTENTS

List of Figures

2.1	CMOS Inverter (a) Schematic diagram (b) Layout design (c) Physical form (in cross-section)	8
2.2	Patterning of silicon dioxide	10
2.3	Design Rules	12
2.4	Two interdigitized transistors	15
2.5	Common centroid arrays. Devices are denoted by letters A and B	16
2.6	Bulk at the ends of transistor	17
2.7	Metal loses its symmetry property after compaction due to symmetry constraints absence	18
2.8	(a) Cascode current mirror (b) Template view	20
2.9	A floorplan representation of an integrated circuit and a symmetry axis marked with dotted line between certain blocks of the circuit.	21
3.1	Symmetry types	25
3.2	Fourier series representation	28
3.3	The symmetry extraction pipeline	30
3.4	Main stages of the proposed algorithm	36
3.5	Building scale space	40
3.6	Different grids used for feature descriptors	42

LIST OF FIGURES

4.1	SIFT Extracted Features are marked by ‘X’	47
4.2	Result of convolution between step function and Gaussian one of different widths w and s respectively.	50
4.3	The circle of the 16 pixels. The pixel p is the center of the candidate corner	51
4.4	FAST Extracted Features are marked by ‘X’	52
4.5	Changes in the intensity with moving the window	53
4.6	Auto-correlation principle curvature	56
4.7	R and M relationship	58
4.8	HARRIS Extracted Features are marked by ‘X’	59
4.9	SIFT corner points extracted with different four scales of NanGate library images	61
4.10	FAST corner points extracted with different four scales of NanGate library images	61
4.11	HARRIS corner points extracted with different four scales of NanGate library images	62
4.12	SIFT, FAST, HARRIS corner points for NOR4_X4	64
5.1	Corner point descriptor consists of four ratio values; two predecessor ratio values to the corner point and two suc- cessor ratio ones respectively.	69
5.2	Matching result of open source SIFT library	71
5.3	Matching result of the proposed algorithm	72
5.4	BUF_X16	74
5.5	NOR4_X4	75
5.6	DFFRS_x2	76
5.7	TBUF_X16	77
5.8	OpampPass - Layer 23	79
5.9	OpampPass - Layer 23	80
6.1	Mapping constraint to metal part in layout	85
6.2	Apply symmetry to the compaction flow of layout	86

LIST OF FIGURES

A.1	Single-crystal ingot cutted into thin slices with wafer saw .	88
A.2	Different operations of photolithography process	89
A.3	Positive and negative photresist	91
A.4	Inverter cross section	92
A.5	Inverter mask set	93
A.6	Masks	94
A.7	Start with blank wafer	94
A.8	Oxidation process where the wafer is covered with SiO_2 .	95
A.9	Photoresist is spinned on the oxide	95
A.10	Lithography where the photoresist is exposed through n-well mask	95
A.11	Oxide exposed is etched with acid	96
A.12	Remaining photoresist stripped off	96
A.13	N-well formed by diffusion or ion implantation	96
A.14	Remaining oxide stripped off using acid	96
A.15	Thin gate oxide layer oxidized then polysilicon layer added	97
A.16	Polysilicon patterning	97
A.17	Expose to n+ dopants using oxide and masking to form nMOS source , drain and nwell contact	97
A.18	N-diffusion	98
A.19	N-diffusion	98
A.20	N-diffusion. Strip off oxide	98
A.21	Similar steps used to form p+ diffusion	99
A.22	Contacts used to wire the devices created by covering with field oxide then etching where contact cuts are needed . . .	99
A.23	Metallization where aluminum is sputtered over the whole wafer and excess metal is removed by patterning leaving wires	100

LIST OF FIGURES
